Graphene-Organic Interfaces
for Vertical Electronic Devices

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Contents

1 Introduction

As electronic devices continue to evolve, there's a growing interest in merging traditional and novel materials to exploit their superior electronic and mechanical properties, develop cost-effective fabrication processes, and enable new functionalities. In this context, a particular interesting combination is that of Graphene (Gr) and Organic Semiconductors (OSCs).[1–5] The unique properties of graphene, a two-dimensional (2D) material celebrated for its exceptional electrical, thermal, and mechanical characteristics,[6–10] combined with the adaptability and versatility of organic semiconductors,[11–14] three-dimensional (3D) materials, present significant promise to overcome some intrinsic limitations of traditional Silicon-based devices. Notably, the rigidity of Silicon and its challenging integration with other materials restricts its use in flexible electronics. In contrast, organic electronic materials that are characterized by their inherent flexibility and ease of integration onto polymeric substrates, present manufacturing advantages including solution processing and large-scale fabrication at low temperature with reduced cost.[13, 15–20] Incorporating graphene into this framework could offer additional advantages, including the field-tunable Gr/OSC barrier height and the realization of vertical architectures with reduced OSC channel length,[3, 21–26] thereby contributing to the development of organic electronic devices. In particular, graphene could help to overcome the limitations imposed by the low conductivity of OSCs and to improve the overall response speed of the devices, potentially unlocking new avenues for flexible electronics operating at high frequencies. However, further research on these mixed-dimensional heterostructures, which are maintained together by van der Waals (vdW) interactions, and advances in the vertical device architectures are still required to meet the demands of future optoelectronic applications such as smart wearables, environmental sensors and flexible displays.

Disseration outline

In this dissertation, I delve into the interfaces formed between graphene and various organic semiconductors, investigating their charge transport characteristics and potential for device integration. **Chapter 2** sets the scientific background by reviewing the relevant literature on hybrid vdW heterostructures and the most promising applications of graphene-organic interfaces for vertical electronic devices, i.e. Vertical Organic Transistors (VOTs). Emphasis is placed on identifying gaps in the current understanding, thus contextualizing the relevance and significance of this research. Properties and charge transport mechanisms critical for the development

of functional applications in organic electronics are highlighted. In **Chapter 3**, the methodologies that are established in this research are outlined. This section provides a step-by-step breakdown of the chemical vapor deposition (CVD) method used to grow graphene on copper foils. The challenges of the wet transfer technique of graphene on Silicon and organic materials, essential for achieving high-quality planar and vertical devices, are detailed. Furthermore, the methods used for depositing the selected organic thin films, ensuring optimal interface quality, are shortly explained. With the focus on reproducibility and quality assessment, other techniques such as Atomic Force Microscopy (AFM) and Raman spetroscopy, used to characterized the fabricated devices, are briefly described. From **Chapters 4 to 7**, the research delves into the experimental results. Adopting state-of-the-art techniques such as AFM and Raman spectroscopy in combination with rigorous electrical characterization methods, these chapters discuss how organic molecules like C60 and Pentacene interact with and influence graphene's electronic properties. Each chapter represents a facet of the broader study, whether it's understanding the effect of molecules on the graphene in-plane charge transport (Chapters 4 and 5), probing the electrical currents across the vertical heterostructures, or exploring temperature-dependent charge carrier injection mechanisms (Chapters 6 and 7).
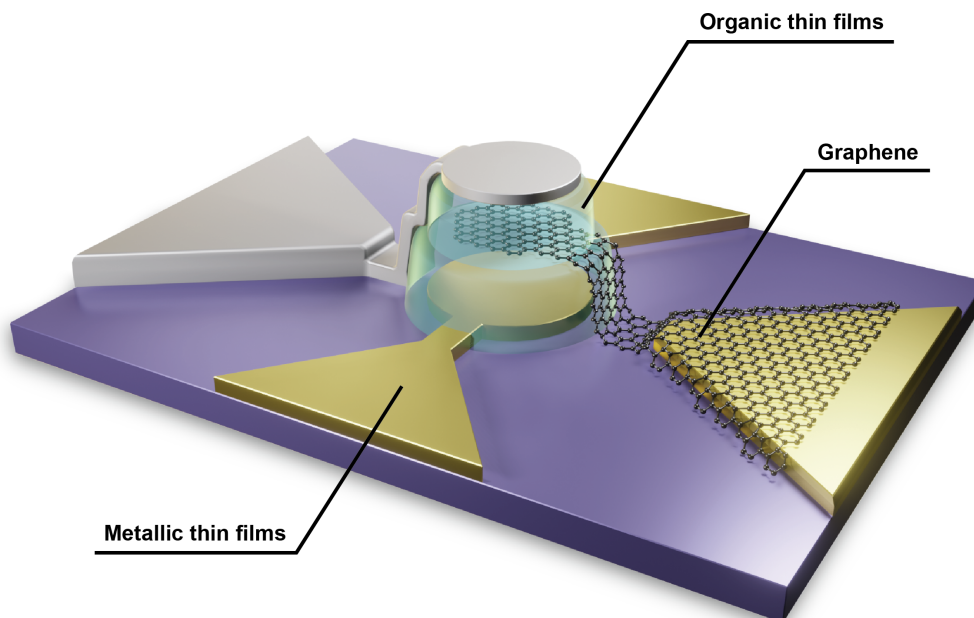
Figure 1: A conceptual illustration of the Vertical Organic Graphene Base Transisor (VOGBT). The device represents the synthesis of the dissertation, aimed at exploring the synergy between the exceptional conductivity and mechanical properties of graphene and the versatility of organic semiconductors for applications in flexible organic electronics.

Chapter 8 extrapolates the acquired knowledge towards tangible applications. It highlights the conceptualization and prototyping approach of a transistor based on Gr/OSC interfaces: the Vertical Organic Graphene Base Transisor (VOGBT), illustrated in Figure 1. The latter has the potential to offer superior performances in terms of gain and frequency response compared to the conventional planar organic transistors and represents a valid alternative to the more recent Vertical Organic Field Effect Transistors (VOFETs). This chapter not only introduces the device but look into its operation principles, performance metrics, and potential for integration into more complex electronic systems. Concluding the body of work, **Chapter 9** provides a reflective analysis. The insights from the previous chapters are consolidated and discussed in the context of their broader impact on the field of electronics. Potential limitations, challenges encountered during the research, and avenues for further exploration and refinement are presented. Overall, by tackling the challenges of fabricating and characterizing various graphene-organic semiconductors interfaces, this dissertation seeks to advance both theoretical understanding and practical applications of graphene in the organic electronics domain.

2 Electronics beyond Silicon

With a focus on flexible organic electronics, the first section highlights the most relevant literature on hybrid van der Waals (vdW) heterostructures. The chapter continues by describing the main electrical properties of Graphene (Gr) / Organic Semiconductor (OSC) interfaces and discusses the potential challenges of their integration into Vertical Organic Transistors (VOTs).

2.1 Hybrid Van der Waals heterostructures

The discovery of graphene in 2004[27] marked a significant milestone in the field of materials science, leading to a strong interest in atomically thin, two-dimensional (2D) materials and their extraordinary properties. These 2D materials offer unique opportunities for the development of advanced optoelectronic devices.[28–30] As research for novel 2D materials continues,[31,32] a particular focus has emerged on layered heterostructures, where multiple 2D crystals are stacked together and held by weak van der Waals (vdW) interactions,[3,33–35] in contrast to other materials, which atoms forms strong covalent bonds with the neighboring atoms, e.g. Silicon. These layered heterostructures not only exhibit novel behaviors in electronics but also provide an alternative approach to the stringent requirements of conventional covalent materials growth, such as epitaxial growth and precise lattice matching.[33,34] Recently, there has been a growing interest in the development of mixed-dimensional heterostructures,[1,3,4,34] where inorganic and organic materials are assembled to create hybrid structures for electronic applications.[33,34,36] These systems explore the combination of zero-dimensional (0D) building blocks, such as inorganic quantum dots and small molecules, and/or one-dimensional (1D) blocks, such as polymers, carbon nanotubes, or nanowires, with 2D crystals. The weak van der Waals interactions play a crucial role in assembling these mixed-dimensional heterostructures, and the exploration of their potential is still in its early stages. Whether focusing on purely 2D stacks or mixed-dimensional heterostructures, the neatness of the surfaces and quality of the interfaces between the constituent materials is of crucial importance.[36] For instance, the processing and transfer methods of graphene expose the interface to contaminants which can prevent reaching high charge carrier mobility.[36,37] Thus, achieving high-performance electronics necessitates precise control and through characterization of these interfaces. In the context of flexible electronics,[38] particularly in Field Effect Transistors (FETs), which typical architecture is shown in Fig. 2a, the absence of an energy gap in graphene reduces its attractiveness compared to other 2D crystals that exhibit true semiconducting be-

havior. However, this drawback becomes less critical in high-frequency applications where graphene's high electronic mobility remains advantageous.[39–44] On the other hand, in recent years, the realization of neat heterostructures has generated interest in electronic devices that leverage the unique vertical geometry of stacked layers (Figs. 2d-e). The weak electrostatic screening exhibited by graphene, due to its low charge carrier density, has greatly influenced the development of vertical field-effect transistors (Fig. 2d).[21] This unique property allows for the tuning of the Schottky barrier at the interface between the semiconductor and graphene, making it an attractive choice for such devices. Consequently, various charge injection mechanisms occurring at the graphene-semiconductor interface, including thermoionic emission,[45,46] Fowler-Nordheim tunneling,[47,48] and trap-assisted tunneling,[49] have been investigated in recent studies. Graphene's role as a semi-permeable membrane for electrons assumes great significance in these systems, further reinforced by the potential to achieve cut-off frequencies up to the terahertz (THz) regime in vertical heterojunctions.[3] In addition, it is worth noticing that the compatibility of graphene with organic compounds holds considerable promise for the development of hybrid electronic heterostructures that integrate organic semiconductor polymers and molecules. This compatibility opens up exciting opportunities for electronic applications which require flexibility and high operational speed.

2.2 Graphene-organic semiconductor interfaces

The implementation of hybrid, mixed-dimensional heterostructures faces a significant obstacle: the current knowledge regarding the graphene-organic semiconductor (Gr/OSC) interface is limited, both in terms of its structural and electronic properties. Despite its potential,[50] the study of this interface and the research on systems combining graphene with organic semiconductors remains relatively scarce,[1,3,22–25,51–53] and a comprehensive understanding is still lacking. This is possibly due to the technical difficulties of integrating these materials, which include compatibility of the fabrication processes and materials stability. Notably, the electronic properties of the graphene-organic semiconductor interface seem to deviate from those of classical metal-semiconductor Schottky diodes.[50] One key characteristic of the Gr/OSC interface arises from the low density of states of graphene at the Dirac point, resulting in a Schottky barrier height that can be tuned by applying an electrical field. This distinctive behavior, referred to as the "barristor" effect,[3,21–26] makes the graphene/semiconductor interface an intriguing platform for studying electronic transport at the interface and exploring potential applications.[21,50] However, further investigation is required to address several unresolved issues. For in-
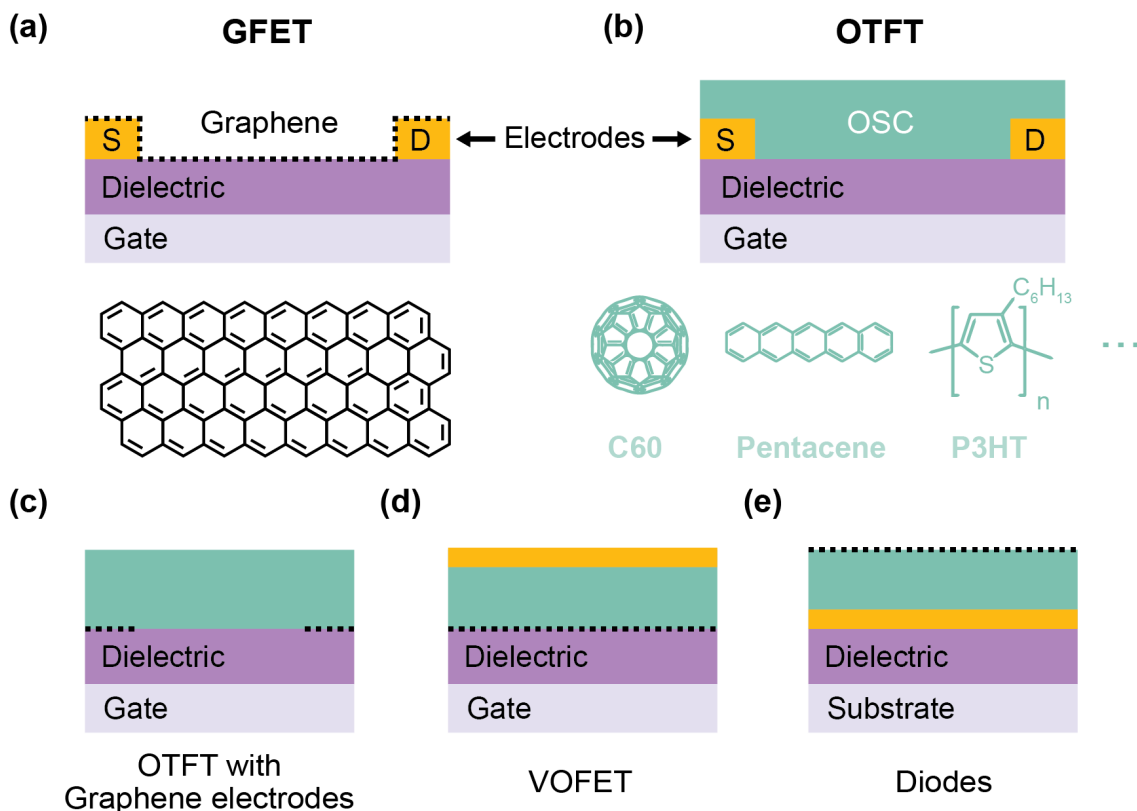
Figure 2:   (a) Schematic of a bottom-gate bottom-contact Graphene Field Effect Transistor (GFET) and chemical structure of graphene (not to scale). (b) Schematic of a bottom-gate bottom-contact Organic Thin Film Transistor (OTFT) and the chemical structures of typical Organic Semiconductor (OSC): the n-type and p-type small molecules C60 and Pentacene, respectively, and the p-type polymer P3HT (not to scale). (c) Illustration of an OTFT implementing graphene as side-contact electrodes. (d) Cross-section of the Vertical Organic Field Effect Transistor (VOFET). (e) Schematic of graphene deposited onto OSCs.

stance, studies have demonstrated that the molecular structure and organization of organic semiconductors differ between OSC/Gr and Gr/OSC structures, particularly for short molecules,[53,54] such as C60 or Pentacene (Fig. 2). However, a systematic comparison of the electronic properties of these two types of interfaces and the influence of molecular organization, is currently lacking. Furthermore, there is limited research regarding polymer-based organic semiconductors, e.g. P3HT (Fig. 2), in relation to the Gr/OSC interface. Another important aspect that requires thorough investigation is the deposition of graphene on organic semiconductors (Fig. 2e), which is far from optimized. Indeed, factors such as the surface roughness of the organic semiconductor may play a role in the variability of the Schottky barrier height values and behaviors. Moreover, the implementation of photolithographic techniques for patterning CVD graphene deposited on organic semiconductors is crucial for the

development of large area fabrication of graphene/organic semiconductor devices. Achieving a detailed understanding of the impact of graphene preparation, surface treatments of organic semiconductors, transfer techniques, and heterostructure formation is essential for the fabrication of high-performances devices.

2.3 Vertical transistors and high frequency
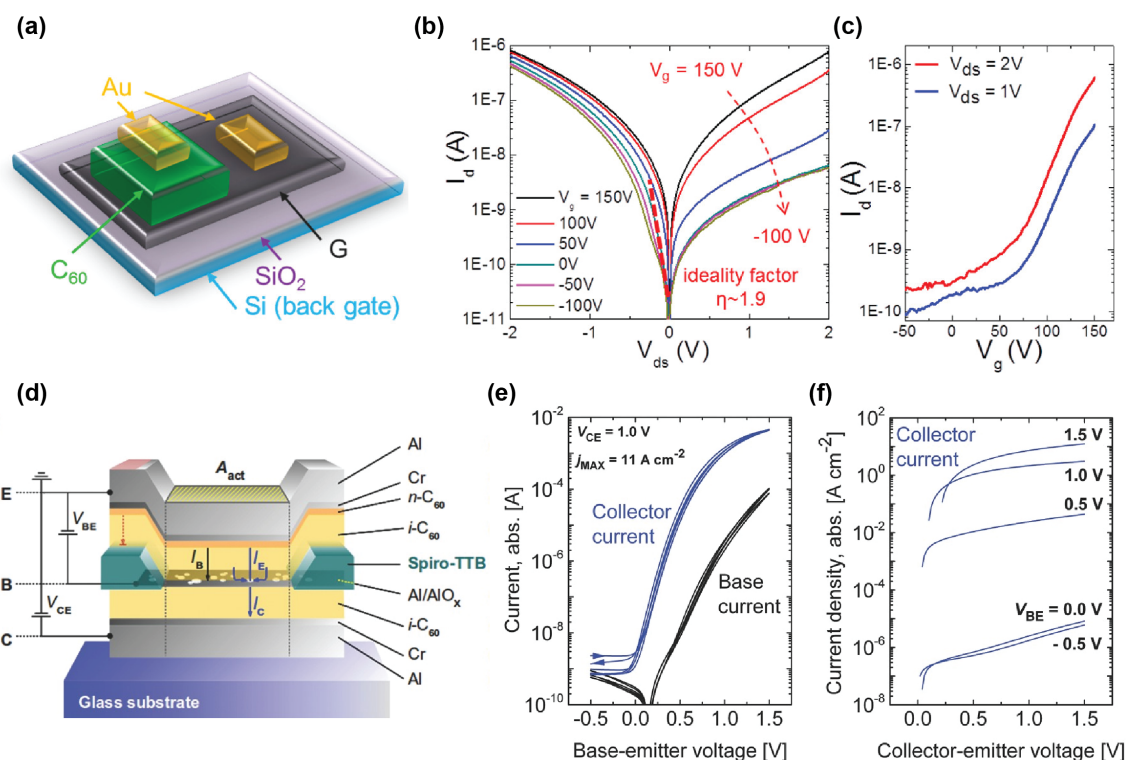
Figure 3: (a-c) Reprinted with permission from K. Kim et Al.[55] ACS Nano. *Copyright © 2015, American Chemical Society.* (a) Device geometry of a C60-graphene vertical structure. (b) Output curve ($I_d - V_{ds}$) with different applied gate voltages V_g. (f) Representative transfer curves ($I_d - V_g$) of a device. (d-f) Reprinted with permission from M.P. Klinger et Al.[56] Adv. Materials. *Copyright © 2015, WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.* (d) A cross-section scheme of the VOPBT. (e) Base sweep of three different VOPBTs with $V_{CE} = 1$ V. (f) Output characteristics, showing that a high on/off ratio is preserved at very low operation voltage.

In organic electronics, vertical organic transistors, which typical configuration is shown in Fig. 2d, represent a valid alternative to traditional horizontal Organic Thin Film Transistors (OTFTs) shown in Figure 2b. The vertical architecture offers the possibility to overcome the limitations of OTFTs, i.e. low transconductance, reduced cut-off frequency, and low integration.[57] While much of the existing literature focuses

on planar OTFT, Vertical Organic Field Effect Transistor (VOFET)[3, 21–26, 55, 58–60] and Vertical Organic Permeable Base Transisor (VOPBT)[56, 61–77] offer a unique advantage. In these two classes of devices, the channel length, is determined by the thickness of the organic semiconductor, which is typically less than 100 nm, in contrast with horizontal devices where the source (S) - drain (D) distance (Fig. 2b) usually ranges from micrometers to tens of micrometers. As a result, vertical organic transistor are expected to achieve higher operational frequencies, which are essential for applications requiring communication and/or data processing functions such as Radio-Frequency (RF) tags, sensors or flexible displays. Figure 3a shows the typical implementation of graphene as a source electrode, for a C60 vertical channel, in VOFET.[55] Figures 3b-c show the output ($I_d - V_{ds}$) and transfer ($I_d - V_g$) characteristics of the device, respectively. When a voltage is applied to the gate electrode, it modulates the charge carrier injection at the Gr/OSC interface, allowing or blocking the current flow between the source and drain electrodes. Although the frequency response of these devices is scarcely investigated, it was recently showed that, a metallic source electrode, in combination with a vertical Dinaphtho[2,3-b:2,3-f]thieno[3,2-b]thiophene (DNTT) short channel, enabled voltage operation below 10 V with a cut-off frequency of 43 MHz.[78] The study also demonstrated that frequencies up to 430 MHz may be achieved by VOFET if the device geometry is finely optimized. With a focus on metal bases, several research groups have explored the VOPBT architecture and its applications.[56, 61–77] A variety of organic semiconductors, both n-type and p-type, have been employed, including C60, perylene derivatives, pentacene, copper phthalocyanine, and poly-hexyl tertiophene. Most of these studies utilized nanoporous aluminum as the base electrode, which has been finely optimized as shown in Figure 3a. In this configuration, the base electrode is placed between two OSCs layers and serves to modulate the current flowing from the emitter to the collector electrodes and across the permeable base electrode. Figures 3e-f show the typical transfer ($I_C - V_{BE}$) and output ($J_C - V_{CE}$) characteristics of such device, respectively. To date, several performance metrics have been reported, showing significant variations in current gains. In certain instances, impressive common emitter gains up to 1×10^8 and high current densities up to $1\,kA/cm^2$ have been observed.[56, 61, 63, 66] In recent years, the device architecture was optimized to reach the transition frequency of 40 MHz in a pulse-biasing mode at $V_{CE} = 8.6\,V$,[79, 80] supporting that VOPBT hold significant promise for high-frequency operation. In addition, device simulations indicate the potential to achieve frequencies in the GHz regime by reducing the thickness of the device and by employing high carrier mobility organic semiconductors.[72] In this context, the unique properties of graphene,

such as ultimate thinness and high conductivity, could further enhance the performance of VOPBT. To the best of our knowledge, there haven't been any published studies on the implementation of graphene as a permeable base electrode such as the Vertical Organic Graphene Base Transisor (VOGBT) illustrated in Figure 1. In this configuration, graphene appears more suitable than metal due to its flexibility and compatibility with low-thermal budget processing. In fact, it has been shown that commonly evaporated metal electrodes can penetrate many tens of nanometers onto the underlying OSC layer.[81] In contrast, the implementation of graphene as top and/or interlayer could enable the reduction of the OSCs stack thickness, potentially, down to organic monolayers. However, deposition and photolithographic patterning methods of CVD graphene compatible with OSCs still need to be developed, and their impact on the structural and electrical properties of the stacks investigated. In particular, the charge transport at the OSC/Gr interfaces will possibly depend on the used OSC and define the functionality of the devices. For instance, a Schottky barrier forming between graphene and the OSC is advantageous when graphene is used as interlayer/base electrode in VOPBT or as top electrode in diodes. Other applications, instead, may require an ohmic contact at the Gr/OSC interface. Finally, it is crucial to ensure that the charge transport mechanisms across the vertical structures are not affected by the lateral dimensions of the devices. This will enable the scaling and further integration of the Gr/OSC stacks into more complex electrical devices that can operate at high frequencies.[70,74,75]

3 Materials and methods

This section describes the Chemical Vapour Deposition (CVD) grown of graphene, the wet transfer method and the deposition of the organic thin films used in this work. The chapter continues with the fabrication processes of the GFETs and of the vertical Graphene (Gr) / Organic Semiconductor (OSC) stacks. A detailed description of the fabrication recipes is reported in Appendix A. The electrical characterization setup, impedance analysis method, Raman microscope and Atomic Force Microscopy (AFM) are also briefly described.

3.1 Chemical vapour deposition of graphene on Cu foils
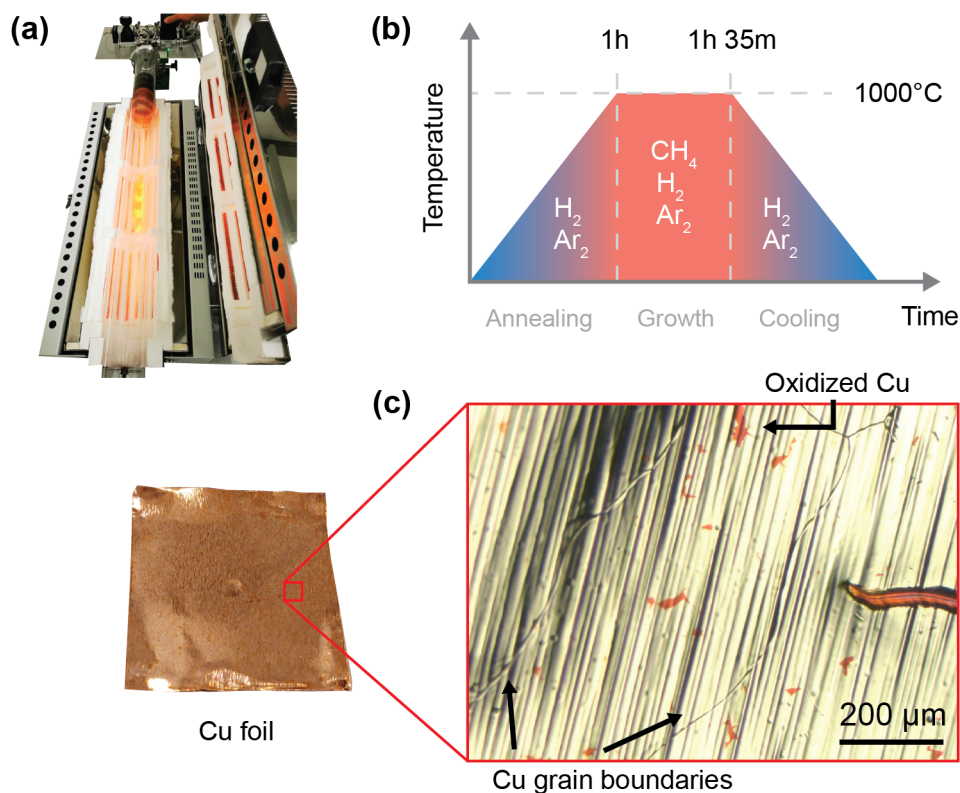
Figure 4: (a) Fully automated Chemical Vapour Deposition (CVD) oven sytem used to grow graphene on copper foils. (b) Temperature vs. Time graph of the CVD growth of graphene. The graph also shows the gases the are used in the different CVD steps: annealing, growth and cooling. (c) Cu foil used as a substrate for the CVD growth of graphene. The optical microscope image shows that graphene is covering a large part of the Cu foil. The uncovered parts of the Cu foil rapidly oxidize when exposed to heat and can be easily distinguished (orange regions).

The Chemical Vapour Deposition (CVD) growth of graphene is shortly reported in previously published articles[82–85] and described in detail here. Graphene was grown

in-house by CVD on copper foils (Thermoscientific, 25 µm thick, annealed, uncoated, 99.8%) with a fully automated setup (Fig. 4a). The foils are ultrasonicated in Acetone, rinsed with Isopropyl Alcohol (IPA) and dried with N_2. Then, the foils are placed in Acetic Acid (CH_3COOH) for 30 min, rinsed in de-ionized water (DIW) and Ethanol, and dried with N_2. The foils are then placed in the CVD oven (Fig. 4a) and the CVD growth process shown in Figure 4b starts. The cleaned foils are pre-annealed at 1000 °C for 1 h in a H_2 (20 sccm) and Ar (200 sccm) atmosphere in the CVD oven (ca. 1 mbar). Then, graphene grows for 35 min in a CH_4 (0.05 sccm), H_2 (20 sccm) and Ar (200 sccm) atmosphere under a pressure of ca. 120 mbar. After the CH_4 flow is stopped, the CVD oven is left to cool down to room temperature (at ca. 1 mbar). Finally, the Cu foils are removed from the CVD oven. The optical microscope image of Figure 4c reveals the typical feaures of the Cu foil surface after the CVD growth. The Cu foil was shortly heated on a hotplate to rapidly oxidize the Cu regions that are not covered by graphene. The change of color occurring due to the oxidation of the exposed Cu regions allows to distinguish the graphene region (white) from the oxidized Cu (orange). Hence, graphene forms a uniform layer on the Cu foils with the exception of small isolated regions. The optical microscope image also shows the Cu grain boundaries. These feature typically results in wrinkles in the transferred graphene,[86] as shown in the next section.

3.2   Transfer of large area graphene from Cu foils to devices

The wet transfer of graphene is reported in previously published articles[82–85] and brifely described here. After the CVD growth, a film of PMMA (50k) was spin-coated on the top side of the CVD graphene/Cu foils to protect graphene during the transfer. Then, the graphene grown on the Cu back side was removed using Reactive ion etching (RIE) in an Ar (15 sccm) and O_2 flow (30 sccm) for 2 min. The Cu substrate was etched away in a Ferric Chloride ($FeCl_3$, Transene CE-100) bath for 1 h, and then transferred to de-ionized water (DIW) as shown in Figures 5a-c. Subsequently, the remaining graphene/PMMA sheet was placed in Hydrochloric acid (HCl 10%) for 5 min to further remove residues of $FeCl_3$[87] and transferred back to DIW. Finally, graphene could be transferred on the target substrate and dried overnight in a vacuum oven (ca. 1 mbar, 80 °C). Figure 5d shows an optical microscope image of graphene on SiO_2 after the removal of the protecting PMMA layer. The typical features of CVD grown graphene can be easily distinguished: (i) the hexagonally shaped grown bilayer (BLG) on top of (ii) the single layer graphene (SLG) and (iii) the wrinkles, which are possibly due to the grain boundaries of the Cu foil used as CVD substrate.[86] These features are highlighted by the G-peak
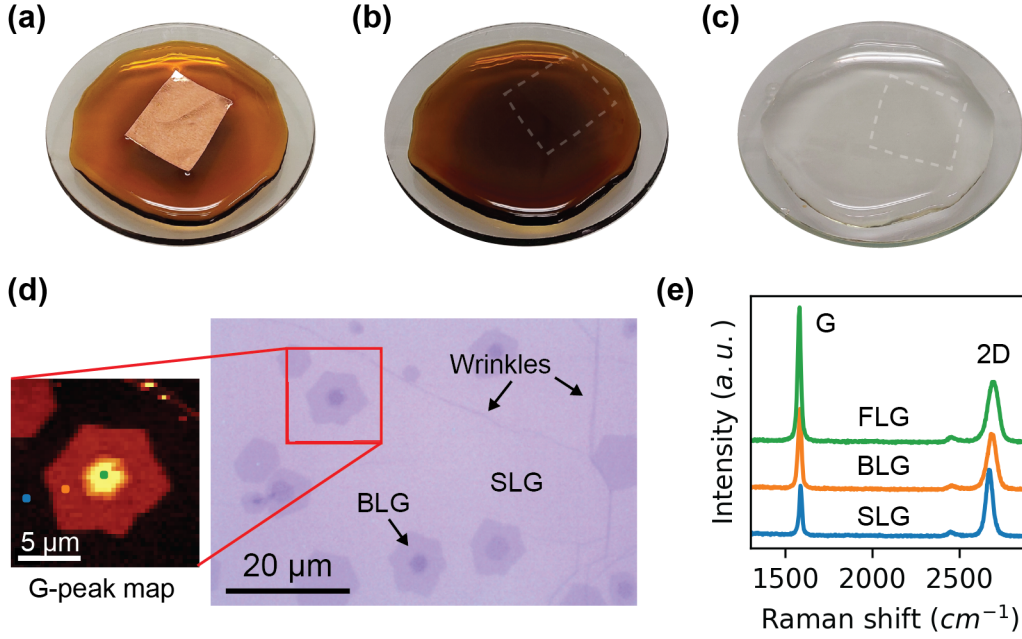
Figure 5: (a) Ferric choride FeCl$_3$ solution (Transene CE-100) etching of the Cu substrate. (b) The Cu foil is completly etched and the remaining graphene/PMMA is floating on the copper etchant. The remaining Gr/PMMA is indicated by the white dashed lines. (c) The Cu etchant is replaced with DIW and HCl 10%. (d) Optical microscope image of graphene transferred on SiO$_2$. The red square indicates the measured Raman map showing the G-peak intensity. (e) Raman spectra of the SLG, the BLG and FLG. The signal acquisition positions are shown in the G-peak map.

map of Figure 5d and by the Raman spectra of Figure 5e. This latter displays the characteristic G (1587 cm^{-1}) and 2D (2681 cm^{-1}) peaks of the CVD graphene on SiO$_2$, obtained using FeCl$_3$ as wet etchant.[88] The absence of the D (around 1340 cm^{-1}) peak suggests that the CVD growth and wet transfer methods did not induce an appreciable quantity of defects in graphene. In addition, the intensity peaks ratios $R = I_G/I_{2D}$ obtained from the Raman spectra in Figure 5e are: $R_{SLG} = 0.96$ for single layer graphene (SLG), $R_{BLG} = 1.06$ for bilayer graphene (BLG) and $R_{FLG} = 1.17$ for few layers (FLG). This indicates that a large area of the Si/SiO$_2$ is covered by SLG.

3.3   Deposition of the organic thin films

Fullerene-C60 (99.9%, sublimed) powder was purchased from Sigma-Aldrich, while Pentacene powder (99.999%, purified by sublimation) was purchased from Tokyo Chemical Industry (TCI). The two types of molecules were thermally evaporated

under vacuum (ca. 1×10^{-6} mbar) without further treatments. The C60 thin film was deposited by thermal evaporation at ca. 0.2Ås^{-1} from a Molybdenum evaporation boat (Umicore). The Pentacene thin film was thermally evaporated at ca. 0.05Ås^{-1} using a low temperature controlled source (ca. 120 °C) with an Al_2O_3 crucible (Creaphys). The temperature of the target substrate wat not actively controlled during the evaporation. poly(3-hexylthiophene-2,5-diyl) (P3HT) (regioregular (RR) > 99%, Mn = 27'000 – 45'000) was purchased from Tokyo Chemicals and used as received to prepare solutions of 10 mg mL^{-1} in chlorobenzene. The P3HT film was deposited by spin-coating at 1000 rpm for 60 s.

3.4   Devices fabrication and characterization
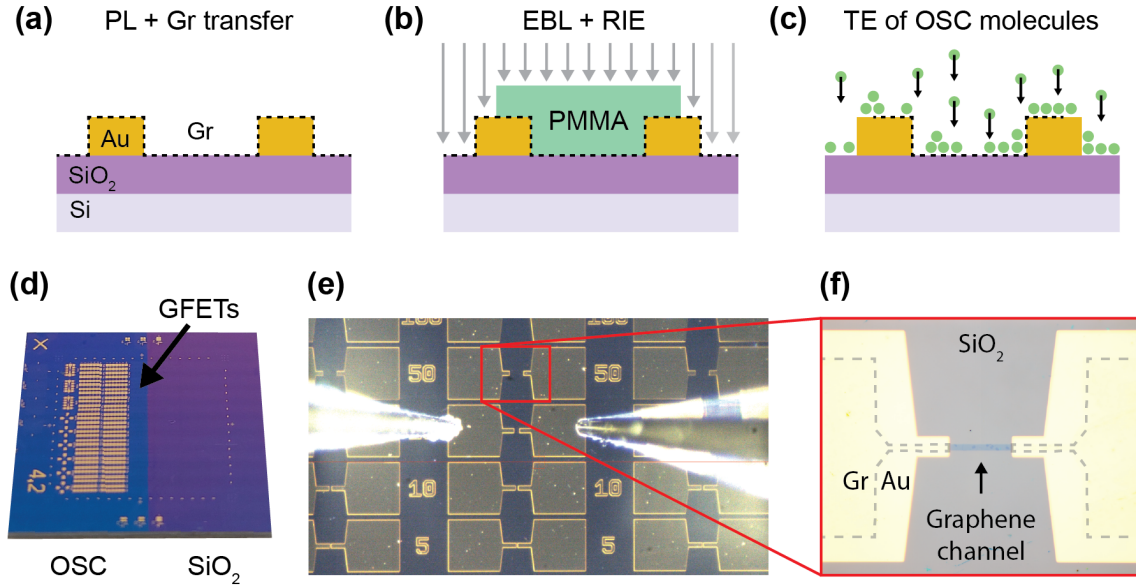
Figure 6: (a) CVD graphene transferred onto photolithography pre-patterned Ti (5 µm) / Au (50 µm) on SiO_2. (b) Ebeam Lithography (EBL) of the protective PMMA layer and RIE patterning of graphene, followed by the removal of the PMMA. (c) Thermal Evaporation (TE) of the organic thin films. (d) Photograph of the fabricated chip including 150 GFETs. (e) Optical microscope image taken with the Automated Probe Station (APS) used to electrically characterize the devices. (f) Zoom-in a GFET with channel length 50 µm and width 5 µm. The grey dashed line shows the outline of graphene overlapping the Au electrodes.

Two chips including 150 Graphene Field Effect Transistors (GFETs) each with a fixed channel width W (5 µm) and five different channel lengths L (5, 10, 20, 50 and 100 µm) were fabricated. Graphene sheets grown by CVD on Cu foils were transferred onto photolithography pre-patterned Ti(5 nm)/Au(50 nm) electrodes on
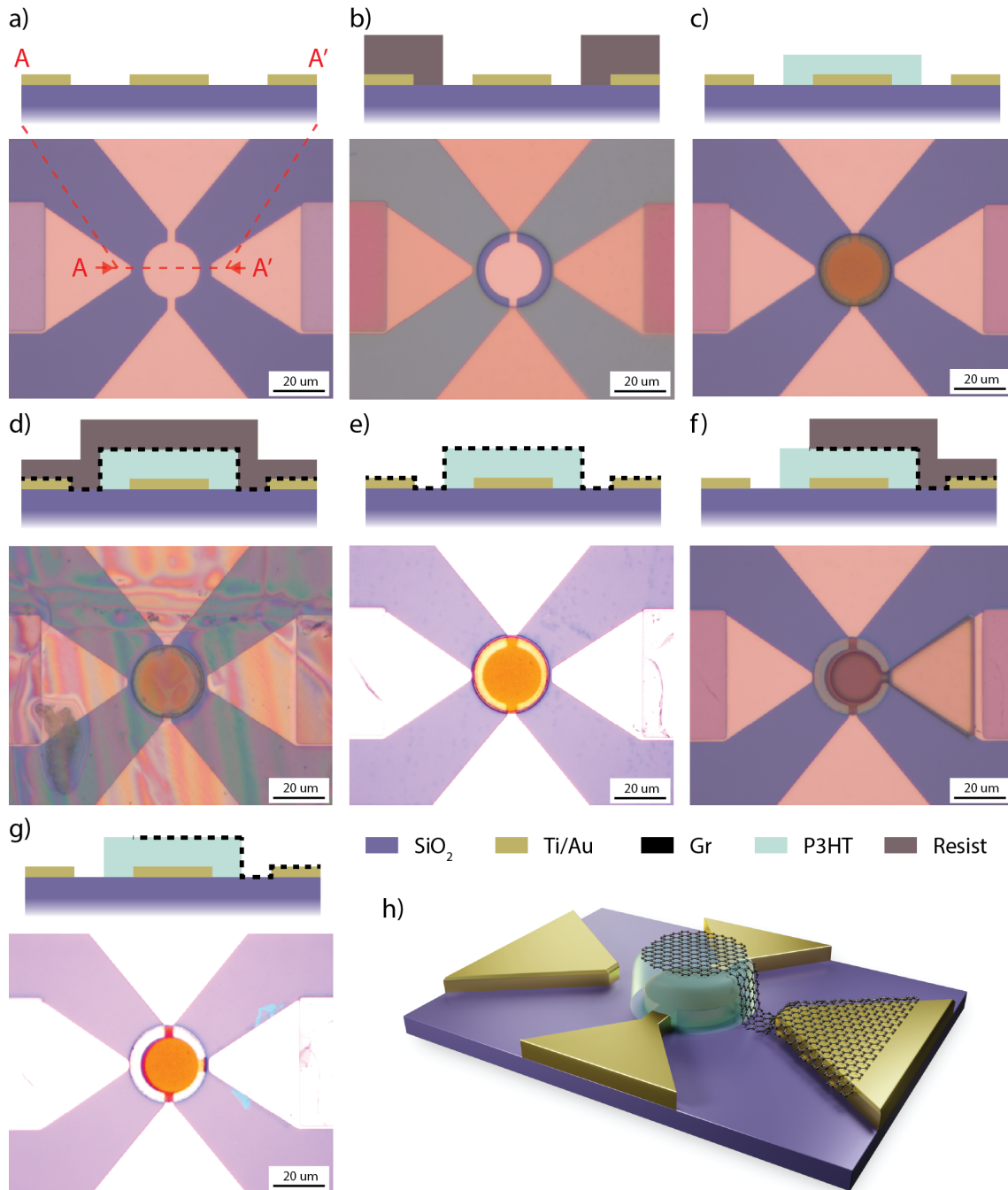
Figure 7: Fabrication steps of the vertical Au / P3HT / Gr heterostructure. (a) Patterning of the bottom electrodes. The grey dashed lines show the schematic of the cross-section (top) on the optical microscope image (bottom). (b) Preparation of the lift-off resist. (c) P3HT deposition and patterning. (d) CVD graphene transfer with PMMA layer. (e) PMMA removal from graphene. (f) RIE patterning of the graphene top electrode. (g) PMMA / Optical resist removal from graphene. (h) 3D schematic of the device.

Si(525 µm)/SiO$_2$(300 nm) substrates. The Au bottom contacts architecture (Figure 6a) was chosen to minimize the number of lithography steps after the transfer of

graphene. A double layer of PMMA 50K/950K (AR-P 632-06 / AR-P 672.02) was spin-coated on graphene, exposed to e-beam and developed for 1 min in MIBK:IPA (1:2). Then, the samples were rinsed in IPA and dried with N_2. Finally, the unprotected graphene was etched away using RIE for 30 s (15 sccm Ar, 30 sccm O_2), as shown in Figure 6b. The remaining PMMA, protecting the graphene channels, was removed in Acetone (55 °C) for 1 h and IPA (55 °C) for 1 h. Finally, thin films of C60 and Pentacene were thermally evaporated on the two separate chips (Figure 6c). Figure 6d shows one chip after the deposition of the organic molecules. The chips were shortly exposed to ambient conditions during the transfer from the evaporation chamber to the vacuum chamber. Figure 6e shows the optical microscope image taken by the Automated Probe Station (APS) used for the electrical characterization. Figure 6f shows the optical microscope image of a representative GFET device with channel length $L = 50 \, \mu m$. The gray dashed line highlights the contour of graphene on top of the Au electrodes.
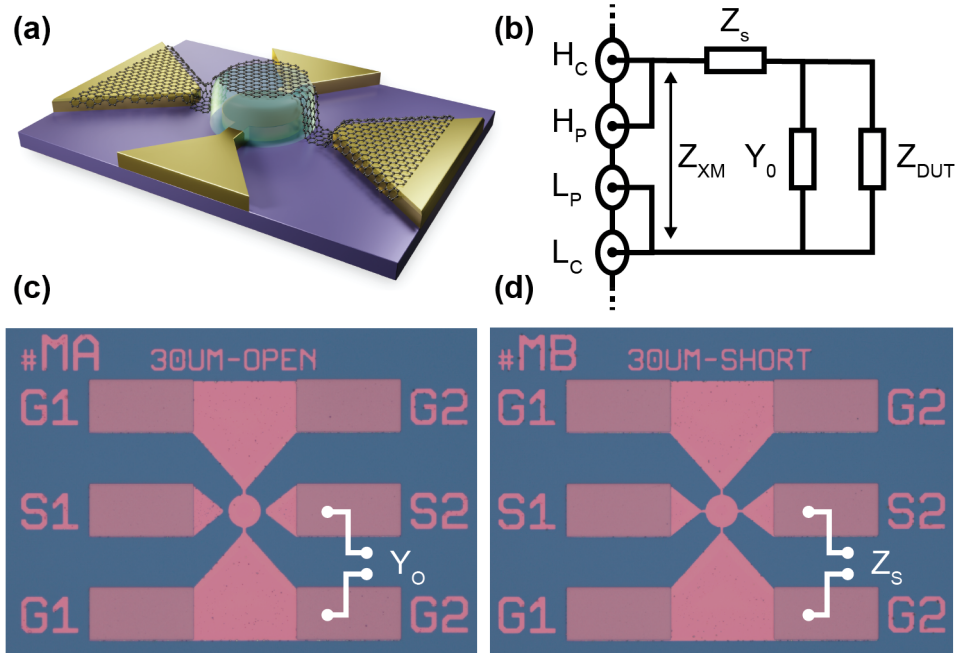
Figure 8:   (a) 3D schematic of a bridge device for the measurement of graphene resistance. (b) Electrical schematic of the open/short compensation for impedance analysis. Adapted from Agilent Impedance Measurement Handbook.[89] Optical microscope images of the (c) open and (d) short compensation devices.

The vertical Au / OSC / Gr devices were fabricated on a Si(525 μm) / SiO$_2$(335 nm) substrate by photolithography and under ambient conditions, as described in Appendix A. The OSC considered for the study were two: P3HT (p-type polymer) and C60 (n-type small molecules). The two systems are discussed in Sections 6 and 7, respectively. The chip includes two distinct groups of devices: (i) 119 Au / OSC / Gr

Vertical Stacks (refer to Figure 23a for a schematic of the device structure) and (ii) 34 Graphene Bridges (Appendix E, Fig. 52). The chips overviews are given in Appendices D and E (Figs. 50 and 64). In both Vertical Stacks and Graphene Bridges, the C60 thin film is sandwiched between a bottom gold and a top graphene circular electrodes. In addition, in the Graphene Bridge architecture (Fig. 8a), graphene is laterally contacted in order to measure its resistance (see Appendix E, Fig. 52, for the electrical scheme). The chip includes devices having graphene electrodes of various nominal diameter, i.e. 5, 10, 15, 20, 25, 30 and 50 µm, while the Au bottom electrodes are 2 µm larger. In short, Au electrodes were pre-patterned and deposited by e-beam physical vapour deposition (EBPVD) and lift-off. Then, the C60 thin film was thermally evaporated ($\approx 0.2\,\text{Ås}^{-1}$, 1×10^{-6} mbar) and patterned by lift-off. Finally, the graphene sheet was wet-transferred on the chip and patterned into the top electrode circular shape by Reactive ion etching (RIE).
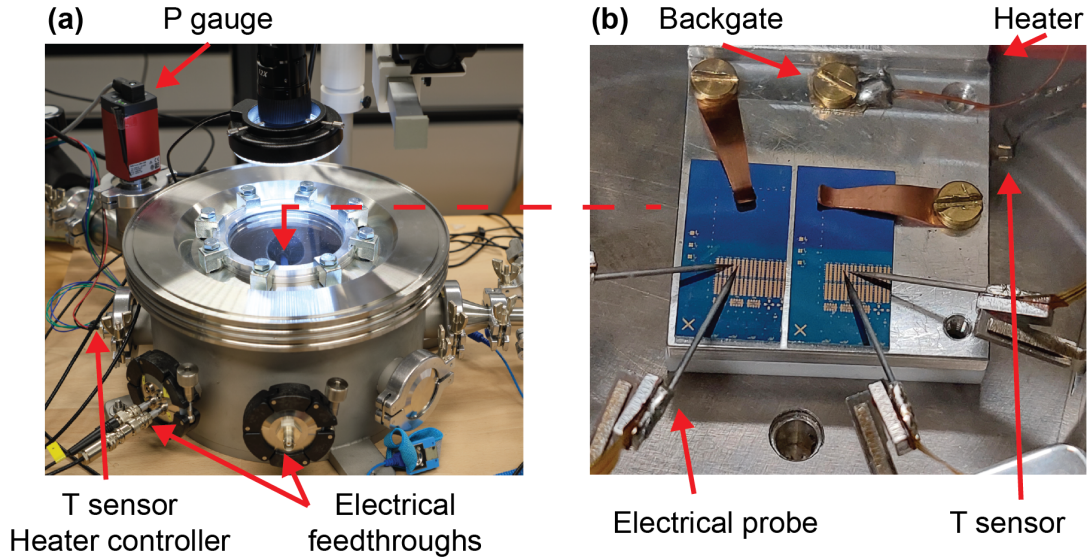
Figure 9:   Measurement setup used for the electrical characterization of the devices. (a) Vacuum chamber containing the electrical probers. The chamber is equipped with a pressure gauge and electrical feedthroughs for the temperature sensor (PT100), the heater power supply, the probes and backgate connectors. (b) Sample holder and electrical probers. The sample order is equipped with a backgate, heater and temperature sensor.

Figure 8b shows the open/short compensation technique used to extrapolate the true impedance of the Device Under Test (DUT).[89] The method consists in measuring the stray admittance Y_0 when the DUT contact terminals are open, and the residual impedance Z_S when the DUT terminals are shorted. To ensure accurate impedance

measurements, open and short devices were fabricated on chip, as shown in Figure 8c and 8d, respectively. The DUT impedance is then calculated from the measured DUT, in formula,[89]

$$Z_{DUT} = \frac{Z_{XM} - Z_S}{1 - (Z_{XM} - Z_S)Y_0} \tag{1}$$

where Z_{DUT} is the corrected DUT impedance, Z_{XM} is the measured DUT impedance, Y_0 is the stray admittance and Z_S is the residual impedance.

The devices were electrically characterized under vacuum to avoid the effects of oxygen and moisture. Figure 9a shows the vacuum chamber, reaching a base pressure of about 1×10^{-6} mbar, that was mainly used for the experiments. The chamber is equipped with a pressure gauge and electrical feedthroughs for the four probers, the sample holder backgate, the heater and the temperature sensors. Figure 9b shows the sample holder that is also employed as backgate for FET measurements. The figure shows the four needles for the electrical probing (IMINA), the electrical connections to the backgate, heater and temperature sensors. The vertical stacks were characterized in the setup showed in Figure 9a-b, the GFETs were characterized in a similar setup equipped with an Automated Probe Station (APS), while the temperature dependent measurements from 50 K to 300 K were performed in a Lakeshore probe station (CRX-6.5K). Refer to the experimental sections for details on the electrical instrumentation and sampling.

3.5   Other characterization methods
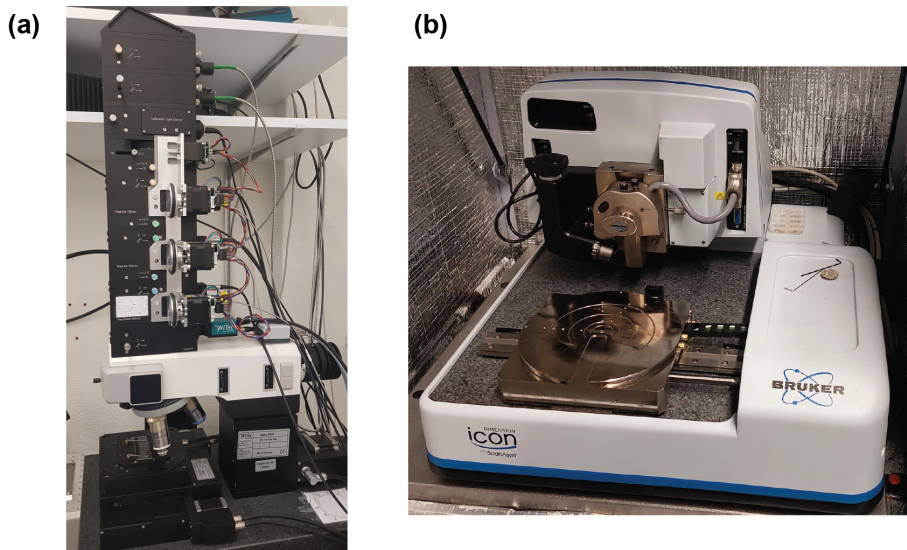
Figure 10:   (a) WITec Alpha 300R confocal Raman microscope. (b) Bruker Atomic Force Microscopy (AFM) Icon equipped with a TESPA-V2 cantilever.

Figure 10a shows the WITec Alpha 300R confocal Raman microscope that was used in this work. The Raman microscope is the ideal non-destructive technique to quickly identify the chemical composition of the Gr / OSC stacks and ensure that the material quality is not compromised during the fabrication process of the devices. The quality of the materials down to the molecular level was evaluated by identifying and comparing the Raman fingerprints of the single components of the vertical stack, i.e. graphene, C60, Pentacene and P3HT. The setup included a LD 100x objective (Zeiss EC Epiplan-Neofluar Dic, NA = 0.75) and a 300 mm lens-based spectrometer (grating: 600 g mm-1) equipped with a TE-cooled charge-coupled device (Andor Newton). The Raman spectra were acquired in ambient conditions using a $532\,\text{nm}$ excitation wavelength, while the laser power and integration time were set according to the measured sample. Refer to the Experimental Methods sections of Chapters 4, 6 and 7 for the specific details on the Raman spectra acquisition and processing on the graphene samples and Gr/OSC devices. Figure 10b shows the Bruker Atomic Force Microscopy (AFM) Icon that was used in this work. AFM is the ideal non-destructive technique that allows for detailed imaging of the surface topology of sensitive materials like graphene and organic molecules. The AFM height and phase images were collected in tapping mode in ambient conditions using a Bruker Icon AFM equipped with a TESPA-V2 cantilever with a tip apex radius of $7\,\text{nm}$ (resonant frequency: $320\,\text{kHz}$, spring constant $37\,\text{N}\,\text{m}^{-1}$).

4 The effect of C60 and Pentacene Adsorbates on the Electrical Properties of CVD Graphene on SiO$_2$

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Jacopo Oswald,[a,b] Davide Beretta,[a] Michael Stiefel,[a] Roman Furrer,[a] Dominique Vuillaume,[d] Michel Calame[a,b,c]. The Effect of C60 and Pentacene Adsorbates on the Electrical Properties of CVD Graphene on SiO2. Nanomaterials 2023, 13 (6), 1134. `https://doi.org/10.3390/nano13061134`.

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Author contributions

Abstract

Graphene is an excellent 2D material for vertical organic transistors electrodes due to its weak electrostatic screening and field-tunable work function, in addition to its high conductivity, flexibility and optical transparency. Nevertheless, the interactions between graphene and other carbon-based materials, including small organic molecules, can affect the graphene electrical properties, and therefore, the device performances. This work investigates the effects of thermally evaporated C60 (n-type) and Pentacene (p-type) thin films on the in-plane charge transport properties of large area CVD graphene under vacuum. This study was performed on a population of 300 graphene field effect transistors. The output characteristic of the transistors revealed that a C60 thin film adsorbate increased the graphene hole density by $(1.65 \pm 0.36) \times 10^{12}\,\mathrm{cm}^{-2}$, whereas a Pentacene thin film increased the graphene electron density by $(0.55 \pm 0.54) \times 10^{12}\,\mathrm{cm}^{-2}$. Hence, C60 induced a graphene Fermi energy downshift of about $100\,\mathrm{meV}$, while Pentacene induced a Fermi energy upshift of about $120\,\mathrm{meV}$. In both cases, the increase in charge carriers was accompanied by a reduced charge mobility, which resulted in a larger graphene sheet resistance of about $3\,\mathrm{k\Omega}$ at the Dirac point. Interestingly, the contact resistance, which varied in the range $200\,\Omega - 1\,\mathrm{k\Omega}$, was not significantly affected by the deposition of the organic molecules.

4.1   Introduction

Hybrid van der Waals (vdW) heterostructures made of Graphene (Gr) and Organic Semiconductor (OSC) are being widely investigated for their potential applications in sensors,[90,91] solar cells,[92] light emitting diodes[93] and vertical transistors.[24,51,52,55,94–97] The latter, which combine very short vertical OSC channels with a graphene electrode, exploit the weak electrostatic screening of graphene and the field-tunable charge injection barrier at the Gr / OSC interface to control the current in the vertical channels. In this context, understanding of the effects of n- and p-type organic molecules at the Gr / OSC interfaces is crucial to enable the realization of efficient graphene-based complementary circuits, the operating mechanisms of which will be limited by graphene conductivity and contact resistance. In fact, the van der Waals interactions of carbon materials, including small organic molecules, e.g. C60-Fullerene and Pentacene, have an important influence on the electrical properties of graphene and therefore, on the device performances. While the growth mechanisms and orientation of C60 and Pentacene molecules on graphene have been widely studied,[55,98–101] a deeper understanding of the Gr / Organic Semiconductor (OSC) interface formation and of the charge transport in graphene is still necessary to achieve desirable electronic device properties and functionalities.

This work investigates the effect of C60 and Pentacene adsorbates on the electrical properties of large-area graphene grown by Chemical Vapour Deposition (CVD). C60 and Pentacene molecules are commonly used as n- and p-type organic semiconductors[1,102,103] that can be thermally evaporated on the target substrate, and are therefore of interest because they can be used for graphene-based complementary circuits. Thin films of C60 and Pentacene were thermally evaporated on two distinct sets of Graphene Field Effect Transistors (GFETs). The surface morphology and chemical composition of the hybrid Gr/C60 and Gr/Pentacene heterostructures, which formed the GFET channels, were investigated using Atomic Force Microscopy (AFM) and Raman spectroscopy. The residual doping and charge carrier mobility in graphene were obtained from the output characteristics of the GFETs in vacuum. Then, the Fermi energy shift induced by the C60 and Pentacene was estimated using the linear energy dispersion relation of graphene. The Transfer Length Method (TLM) was used to extrapolate the sheet and contact resistance of graphene. Finally, the electrical properties of graphene before and after the deposition of the C60 and Pentacene molecules were compared and summarized.

4.2 Results and Discussion
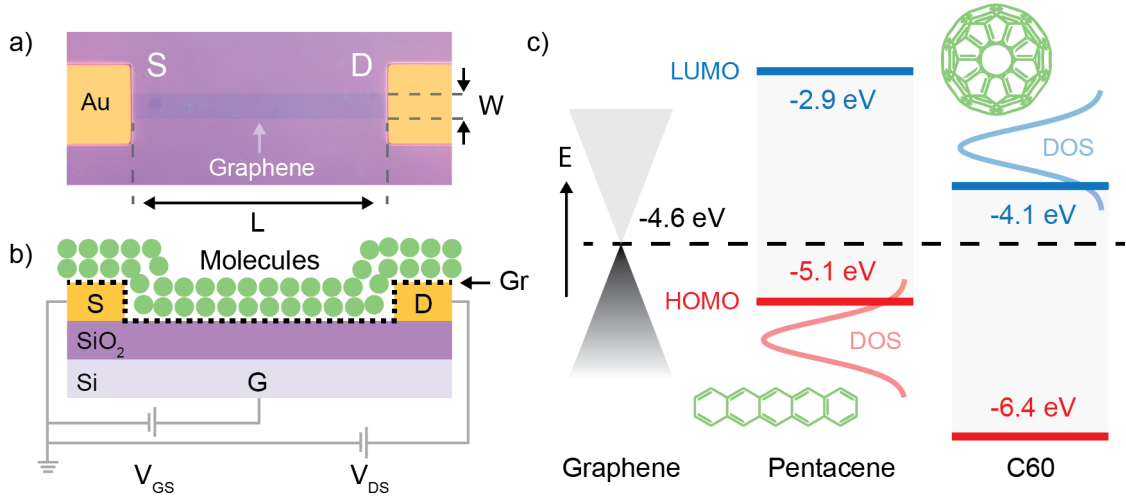
Figure 11: (a) Optical microscope image of a representative Graphene Field Effect Transistor (GFET). The channel length L and width W are $50\,\mu m$ and $5\,\mu m$, respectively. The image shows the source (S) and drain (D) gold electrodes on the Si/SiO$_2$ substrate. (b) Electrical schematic of the GFET (not to scale). The cross-section shows the heavily p-doped Si Gate (G), the SiO$_2$ dielectric ($300\,nm$), the Ti/Au source/drain ($5\,nm/50\,nm$) and the Gr channel coated with C60 and Pentacene molecules. The source (S) electrode is connected to ground. In the gate-to-source voltage (V_{GS}) sweep, the drain-to-source bias (V_{DS}) is kept constant while the current (I_{DS}) is measured. (c) Energetic represenation of the highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO) nominal levels of the C60 and Pentacene molecules with respect to the Fermi energy level of pristine graphene (black dashed line). The Fermi energy of graphene lies within $0.5\,eV$ from the HOMO energy level of Pentacene and within $0.5\,eV$ from the LUMO energy level of C60.

This study was performed on two sets of 150 Graphene Field Effect Transistors (GFETs) each with a fixed channel width W ($5\,\mu m$) and five different channel lengths L (5, 10, 20, 50 and $100\,\mu m$). The two sets include 30 GFETs per channel length and were fabricated on separate chips (Figure 32). The detailed fabrication protocol of the two chips and the Chemical Vapour Deposition (CVD) process used to grow the graphene sheets are reported in the Experimental Methods section. Briefly, the Cu foil that is used as substrate for the CVD growth of graphene is etched away using Ferric Chloride (FeCl$_3$). The remaining graphene sheet was transferred on the pre-patterned Ti/Au electrodes ($5\,nm/50\,nm$) on a Si/SiO$_2$ ($525\,\mu m/300\,nm$) substrate and patterned into geometrically defined channels by e-beam lithography. Then,

molecules were thermally evaporated, without using any physical masks nor photolithographic patterning, resulting in a uniform coverage of the whole chip. Figure 11a shows the optical microscope image of a representative GFET with $L = 50\,\mu m$ and $W = 5\,\mu m$. The output and transfer characteristics of the GFETs were measured in vacuum before and after depositing the molecules, after $24\,h$ of vacuuum exposure to assure complete desorption of the moisture and water. Figure 11b shows the electric circuit and cross-section schematics of a GFET coated with C60 or Pentacene. Figure 11c shows the highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO) energy levels of the two Organic Semiconductors (OSCs) and the Fermi energy of graphene, i.e. $-4.6\,eV$, with respect to the vacuum level, according to the literature.[1] The reported values of the HOMO and LUMO energy levels of C60 are about $-6.4\,eV$ and $-4.1\,eV$,[1,104] while for Pentacene, they are about $-5.1\,eV$ and $-2.9\,eV$, respectively.[1,105,106] The HOMO and LUMO energy levels of the OSCs were extrapolated from Ultraviolet Photoelectron Spectroscopy (UPS) and Inverted Photoelectron Spectroscopy (IPES) measurements, and defined at the onset of the GaussianDensity of States (DOS),[105] as roughly shown in Figure 11c for an arbitrary Gaussian distribution. The Fermi energy of graphene lies within about $0.5\,eV$ from the HOMO energy level of Pentacene and within about $0.5\,eV$ from the LUMO energy level of C60. Accordingly, one would expected that C60 and Pentacene adsorbates act like electron acceptors and donors, which are well suited for the investigation of the p- and n-type induced charge carrier density in graphene. However, the energetic of the interfaces is not trivial, and many factors can play a role, including (i) intragap defects, which could result in occupied and unoccupied states, (ii) dipole formation, (iii) Fermi-level pinning, and/or (iv) the presence of impurities, e.g. , H_2O and/or resist residues.[107–112] Therefore, the effect of the adsorbates on the graphene properties cannot be forecasted by simple arguments on the energy diagrams of the isolated systems. On the other hand, one can estimate the residual charge density from the transfer characteristics of the GFETs in a controlled environment. In addition, a combination of Raman spectroscopy and Atomic Force Microscopy (AFM) gives important insight on the morphology and chemical composition of the Gr / OSC hybrid heterostructure.
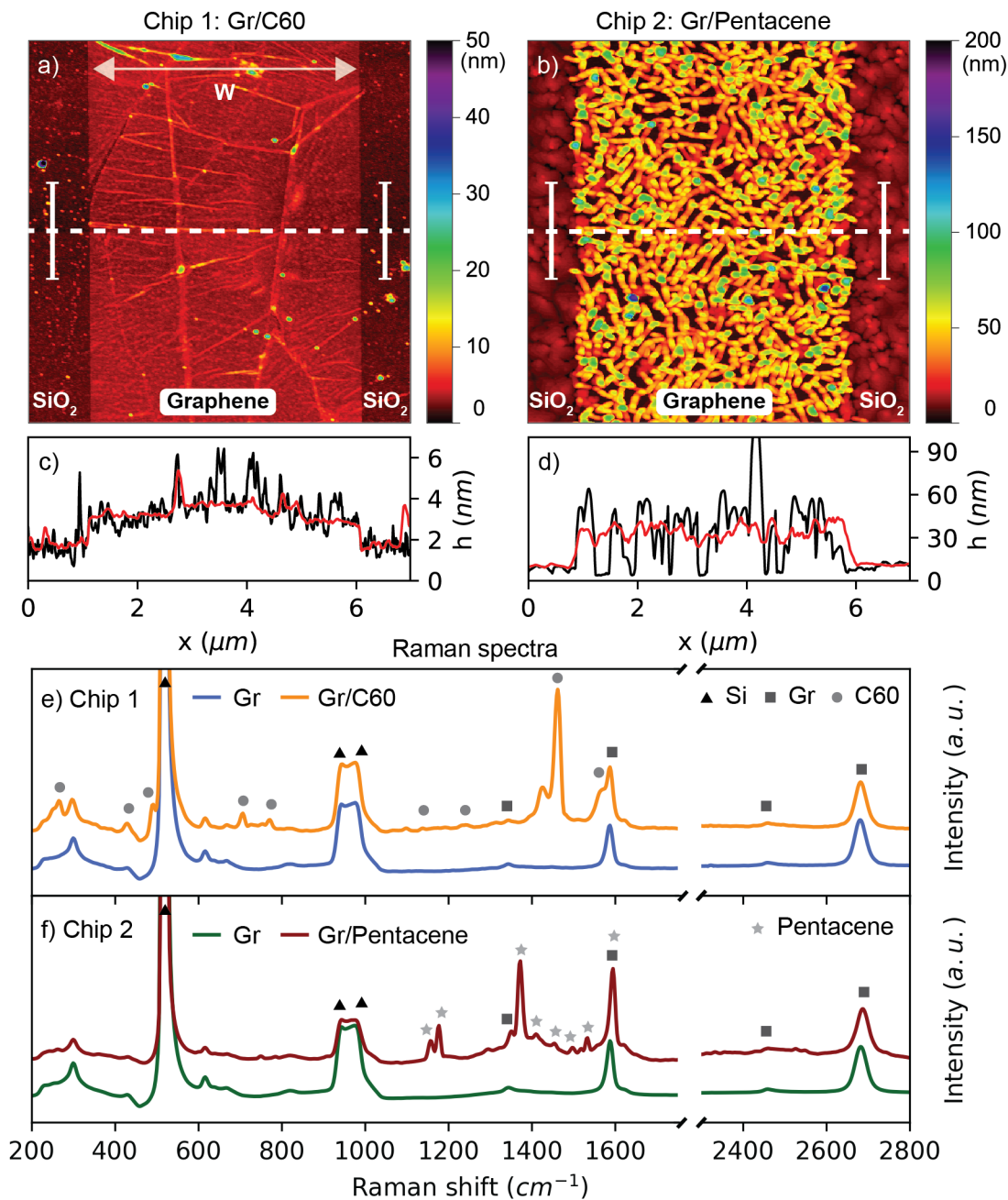
Figure 12:   Surface morphology and chemical composition of the Gr / C60 (Chip 1) and Gr / Pentacene (Chip 2) heterostructures. (a) AFM height image of a represenative Gr / C60 FET channel. (b) AFM image of a represenative Gr / Pentacene FET channel. (c) AFM height profile (black line) of the Gr / C60 channel taken along the dashed white line in (a). The red line is the mean value of 128 height profiles shown by the white bars in the AFM image. (d) AFM height profile of the Gr/Pentacene channel taken along the dashed white line in (b). (e) Average Raman spectra of the C60-GFETs (Chip 1). The Raman spectrum of the pristine CVD graphene is blue, while the Raman spectrum of Gr / C60 is orange. (f) Average Raman spectra of the Pentacene-GFETs (Chip 2).

Figure 12: The Raman spectrum of the pristine CVD graphene is green, while the Raman spectrum of Gr / Pentacene is red. All spectra are normalized to the 2D peak of graphene. The triangle, sqaure, circle and star symbols represent the characteristic Raman peaks of Si,[113] Gr,[88] C60[114] and Pentacene,[115] respectively.

Figure 12a-b shows the AFM images and profiles of two representative GFET channels coated with thin films of C60 (Chip 1) and Pentacene (Chip 2), respectively. The average measured thickness of the C60 and Pentacene layers on the SiO_2 substrates were about 10 nm and 5 nm, as shown in the Supplementary Materials (Figure 32a-d). The height difference and morphology were attributed to the different growing mechanisms of C60 and Pentacene on SiO_2 and graphene. The AFM profile of Figure 12c reveals a uniform C60 thin film growth on both SiO_2 and graphene, as was previously reported.[55] The average height step of about 1 nm (red line) on the GFET channel was due to graphene, and it was in the range of previously reported values for pristine graphene, i.e., 0.4 nm–1.7 nm.[116] The discrepancy between the measured and expected step thickness of graphene (about 0.3 nm) was therefore not surprising and could be attributed to different components, including the graphene-adsorbate layer, tip-surface interactions and imaging force.[116] Here, the very thin layer of C60 allowed for the observation of the typical features of the underlying CVD graphene sheet (e.g., wrinkles caused by the Cu catalyst grain boundaries[86]). The AFM image of Figure 12b shows that thermally evaporated Pentacene grew in the typical thin film phase on SiO_2,[115] whereas it grew in 3D elongated islands on graphene.[98,100] Figure 12d shows that the average channel step thickness was approximately 30 nm (red line), and that the Pentacene film on graphene formed an irregular profile (black line) of 30-50 nanometer-thick elongated islands. The thick Pentacene islands masked the typical features of the underlying CVD graphene, which were not visible in the AFM image. Nevertheless, the graphene channel was clearly distinguishable due to the different growth mechanisms of Pentacene on SiO_2 and on the graphene channel. The presence of the graphene channel under the organic thin films was further confirmed using Raman spectroscopy. Figure 12e-f shows the average Raman spectra obtained from each set of 150 devices before and after deposition of the thin films. Refer to the Experimental Methods section and the Supplementary Materials (Figures 33 and 34) for the details on the Raman signal acquisition, averaging, background subtraction and normalization. The Raman spectra of wet transferred CVD graphene (Gr on Si/SiO_2 substrate) showed the characteristic G ($1587\,cm^{-1}$) and 2D ($2681\,cm^{-1}$) peaks, as well as the D ($1340\,cm^{-1}$) peak,[88] with a weak amplitude, possibly resulting from fabrication-induced defects. The typical first-order optical

mode ($520\,\mathrm{cm^{-1}}$) and second-order scattering band ($940\,\mathrm{cm^{-1}}$–$980\,\mathrm{cm^{-1}}$) of the Si substrate[113] were observed in all Raman spectra. Figure 12e shows the chemical composition of the GFETs (Chip 1) before (Gr) and after (Gr/C60) the deposition of C60. The hybrid Gr/C60 layer displayed the characteristic Raman active vibrations of C60,[114] i.e., H_{1g} at $264\,\mathrm{cm^{-1}}$, H_{2g} at $430\,\mathrm{cm^{-1}}$, A_{1g} at $491\,\mathrm{cm^{-1}}$, H_{3g} at $707\,\mathrm{cm^{-1}}$, H_{4g} at $772\,\mathrm{cm^{-1}}$, H_{5g} at $1099\,\mathrm{cm^{-1}}$, H_{6g} at $1242\,\mathrm{cm^{-1}}$, A_{2g} at $1462\,\mathrm{cm^{-1}}$ and H_{8g} at $1568\,\mathrm{cm^{-1}}$, as well as the characteristic Raman peaks of CVD graphene (G at $1587\,\mathrm{cm^{-1}}$ and 2D at $2681\,\mathrm{cm^{-1}}$) observed before the deposition of C60. Figure 12f shows the chemical composition of the GFETs (Chip 2) before (Gr) and after (Gr/Pentacene) the deposition of Pentacene. The hybrid Gr/Pentacene layer showed the characteristic Raman features of Pentacene.[117] The peaks at 1158, 1177, 1371, 1410, 1456, 1499 and $1533\,\mathrm{cm^{-1}}$ were assigned to the A_g bands, while the peak at $1595\,\mathrm{cm^{-1}}$ was assigned to the B_{3g} band. The 2D peak ($2687\,\mathrm{cm^{-1}}$) of the CVD graphene could be clearly distinguished, whereas the G peak overlapped with the B_{3g} band of Pentacene. The AFM surface morphology combined with Raman chemical analysis confirmed the presence of the geometrically well-defined Gr/C60 and Gr/Pentacene hybrid heterostructures.
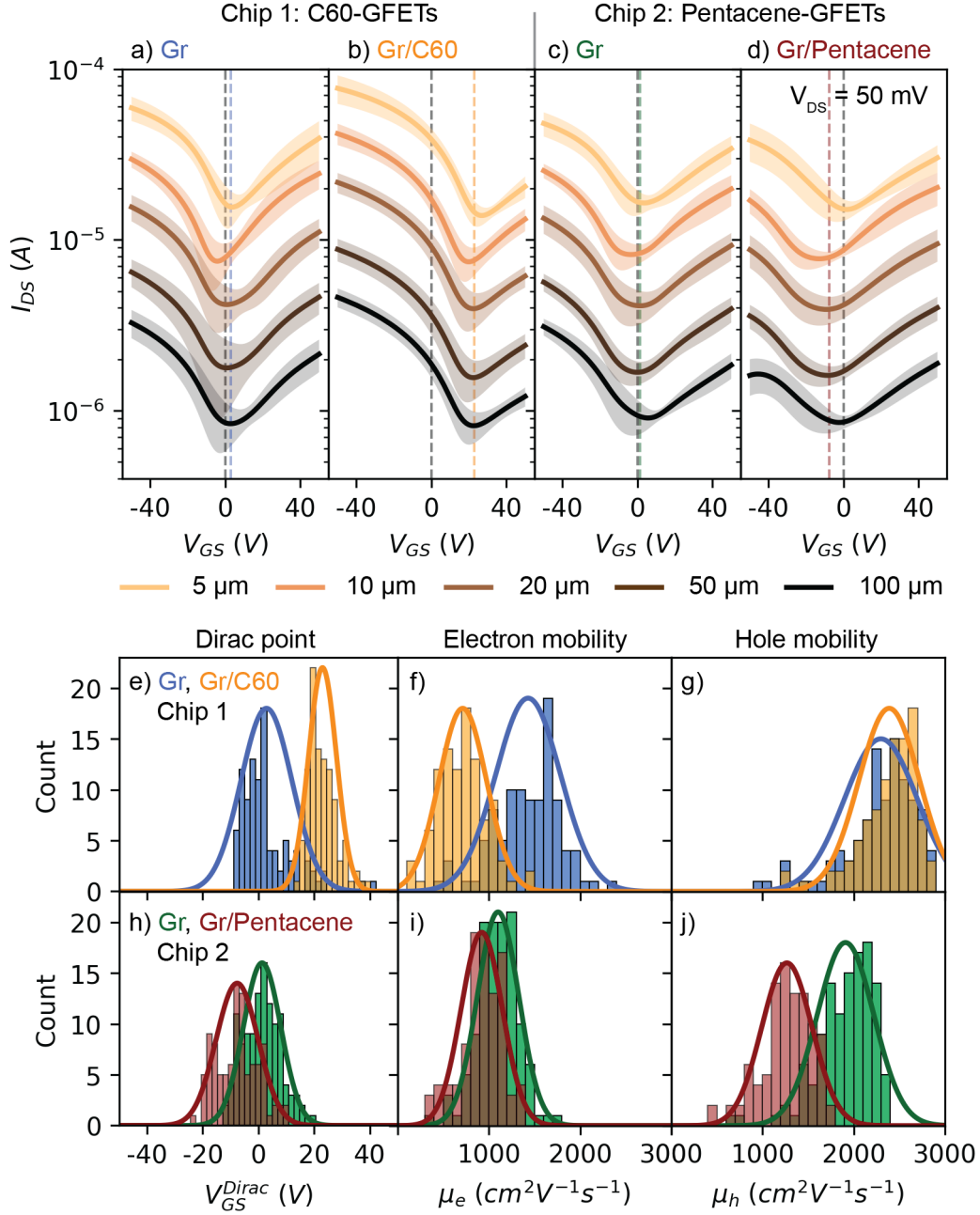
Figure 13: GFETs electrical measurements. (a) Average transfer characteristic (I_{DS} vs. V_{GS}) of pristine CVD graphene FETs before C60 deposition (Chip 1, 101 devices, all L included). The shaded areas are the standard deviations. (b) Average transfer characteristic of the C60-GFETs (Chip 1, 101 devices, all L included). (c) Average transfer characteristic of pristine CVD graphene before Pentacene deposition (Chip 2, 119 devices, all L included). (d) Average transfer characteristic of the Pentacene-GFETs (Chip 2, 98 devices, all L included). (e) Histograms of the graphene Dirac position (V_{GS}^{Dirac}) before (blue) and after deposition of C60 (orange). (f) Histograms of the graphene electron mobility (μ_e) before (blue) and after deposition of C60 (orange), all L included. (g) Histograms of the graphene hole mobility (μ_h) before (blue) and after deposition of C60 (orange), all L included.

Figure 13: (h) Histograms of the graphene Dirac position (V_{GS}^{Dirac}) before (green) and after deposition of Pentacene (red), all L included. (i) Histograms of the graphene electron mobility (μ_e) before (green) and after deposition of Pentacene (red), all L included. (j) Histograms of the graphene hole mobility (μ_h) before (green) and after deposition of Pentacene (red), all L included. Bins width of graphene Dirac point position and mobility histograms are $2\,\mathrm{V}$ and $100\,\mathrm{cm^2V^{-1}s^{-1}}$, respectively.

Figure 13a-d show the average transfer characteristics (I_{DS} vs. V_{GS}) of pristine GFETs and coated GFETs measured under vacuum and at room temperature. The standard deviations are indicated by the shaded areas. Refer to the Experimental Methods section for the details on the data selection and to the Supporting information for all the individual output characteristics (Figure 35), transfer characteristics (Figure 36) and information on the population (Figure 3). All the devices show the typical output characteristic (I_{DS} vs. V_{DS}) and transfer characteristic (I_{DS} vs. V_{GS}) of graphene field effect transistors,[39] The transfer characteristics displayed negligible hysteresis (Figure 36), and thus only the continuous backward traces were considered. All C60-GFETs (Chip 1) showed $I_G \ll I_{DS}$ on the entire V_{GS} (Figure 37), while all Pentacene-GFETs displayed a pronounced gate-leakage at high negative gate voltages, a phenomon that does not affect the conclusion of this work. As expected, the I_{DS} was inversely proportional to the graphene channel length L ($I_{DS} \approx 1/L$) and the position of the Dirac point V_{GS}^{Dirac}, which corresponds to the minimum of the I_{DS}, was found at positive and close to zero V_{GS} for the two sets of pristine GFETs, i.e. $V_{GS}^{Dirac} = 2.8 \pm 9.1$ V for Chip 1 and $V_{GS}^{Dirac} = 1.3 \pm 6.7$ V for Chip 2. This indicates that the fabrication process resulted in clean graphene, possibly with few PMMA resist residues and thus a relatively low p-doping level.[107–110] Figures 13b and 13d show that the distribution of the Dirac point of the GFETs was shifted to $V_{GS}^{Dirac} = 23.0 \pm 5.0$ V after the deposition of C60 (Chip 1), while it was shifted to $V_{GS}^{Dirac} = -7.6 \pm 7.5$ V after the evaporation of Pentacene (Chip 2). Assuming that the Dirac point position shift was solely due to the charge transfer between graphene and the molecules, it was possible to estimate the residual doping in graphene. In fact, the relation between the charge carrier density n in the graphene channel and V_{GS}, neglecting the quantum capacitance,[39,118] is given by the electrostatic capacitance. In Formula,[110]

$$n = \frac{C_{GS}}{e}|V_{GS} - V_{GS}^{Dirac}| \tag{2}$$

where e is the elementary charge and $C_{GS} = (\epsilon_0\epsilon_r)/t$ is the gate capacitance per unit

area, where ϵ_0 is the vacuum permittivity, while $\epsilon_r = 3.9$[119] and $t = 300\,\text{nm}$ are the dielectric constant and thickness of SiO_2, respectively. Therefore, the residual doping in graphene due to the molecules is given by $n_0 = n(V_{GS} = 0)$. When $V_{GS} > V_{GS}^{Dirac}$), electrons are accumulated in the graphene channel, while for $V_{GS} < V_{GS}^{Dirac}$), holes are accumulated in the graphene channel. The deposition of C60 molecules led to a graphene hole-density of $n_0 = (1.65 \pm 0.36) \times 10^{12}\,\text{cm}^{-2}$, against the residual doping of pristine graphene of $n_0 = (0.20 \pm 0.65) \times 10^{12}\,\text{cm}^{-2}$ (Chip 1). For the Pentacene molecules, the graphene was electron doped with an electron-density of $n_0 = (0.55 \pm 0.54) \times 10^{12}\,\text{cm}^{-2}$, against the residual hole doping of graphene before the deposition of $n_0 = (0.09 \pm 0.48) \times 10^{12}\,\text{cm}^{-2}$ (Chip 2). Such a charge transfer could not be anticipated a priori from the HOMO or LUMO energy level of the individual molecules relative to the graphene Fermi level only, as illustrated for C60 and Pentacene in Figure 11c. The corresponding graphene Fermi level shift, at $V_{GS} = 0$ V, could be extrapolated from the linear energy dispersion relation of graphene,[7] i.e. $\Delta E = E_{DP} - E_F = -sgn(V_{GS}^{Dirac})\hbar v_F \sqrt{\pi n_0}$. Where E_{DP} is the energy of the Dirac point, $E_F = -4.6\,\text{eV}$ is the Fermi energy and $v_F = 1 \times 10^6\,\text{m\,s}^{-1}$ is the Fermi velocity in graphene. The deposition of C60 on graphene resulted in a Fermi energy downshift of $\Delta E = -150 \pm 15$ meV, against $\Delta E = -52 \pm 55$ meV for the pristine graphene (Chip 1). The deposition of Pentacene on graphene resulted in a Fermi energy upshift of $\Delta E = 86 \pm 35$ meV, against $\Delta E = -36 \pm 53$ meV for pristine graphene (Chip 2). The charge carrier density n_0 and Fermi energy shift ΔE induced by C60 on graphene were similar to previously reported values for Gr/C60 hybrid layers obtained from Raman and THz-TDS measurements.[120] The field effect transistor measurements, compared to other techniques, allow to determine both the hole mobility μ_h and electron mobility μ_e from a single V_{GS} sweep. In fact, the field effect electron and hole mobility reads,[39]

$$\mu = \frac{L g_m}{W C_{GS} V_{DS}} \tag{3}$$

where $g_m = max(dI_{DS}/dV_{GS})$ is the maximum transconductance at $V_{DS} = 50\,\text{mV}$.[83] The hole mobility and electron mobility were obtained from the transfer characteristics for $V_{GS} < V_{GS}^{Dirac}$ and for $V_{GS} > V_{GS}^{Dirac}$, respectively. Refer to the Experimental methods and Supporting information (Figure 38) for the details on the numerical derivative of the I_{DS} vs. V_{GS} traces. Figure 13e-j show the distributions of the Dirac point V_{GS}^{Dirac}, the electron mobility μ_e and hole mobility μ_h of the GFETs before and after the deposition of the molecules. In the C60-GFETs measurements (Chip 1), the increase of the residual hole-density n_0 was accompanied by a decrease, from

$\mu_e = 1430 \pm 354 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ to $\mu_e = 713 \pm 261 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, of the electron mobility, possibly due to an increased charge-impurity scattering.[121] The hole mobility remained almost unaffected, as shown in Figures 13f and 13g. Similarly, the deposition of Pentacene on the GFETs (Chip 2), led to an increase of the residual electron-density n_0 which was accompanied by a decrease, from $\mu_h = 1910 \pm 310 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ to $\mu_h = 1268 \pm 275 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, of the hole-mobility. The electron-mobility is also slightly reduced, as shown in Figures 13i-j.
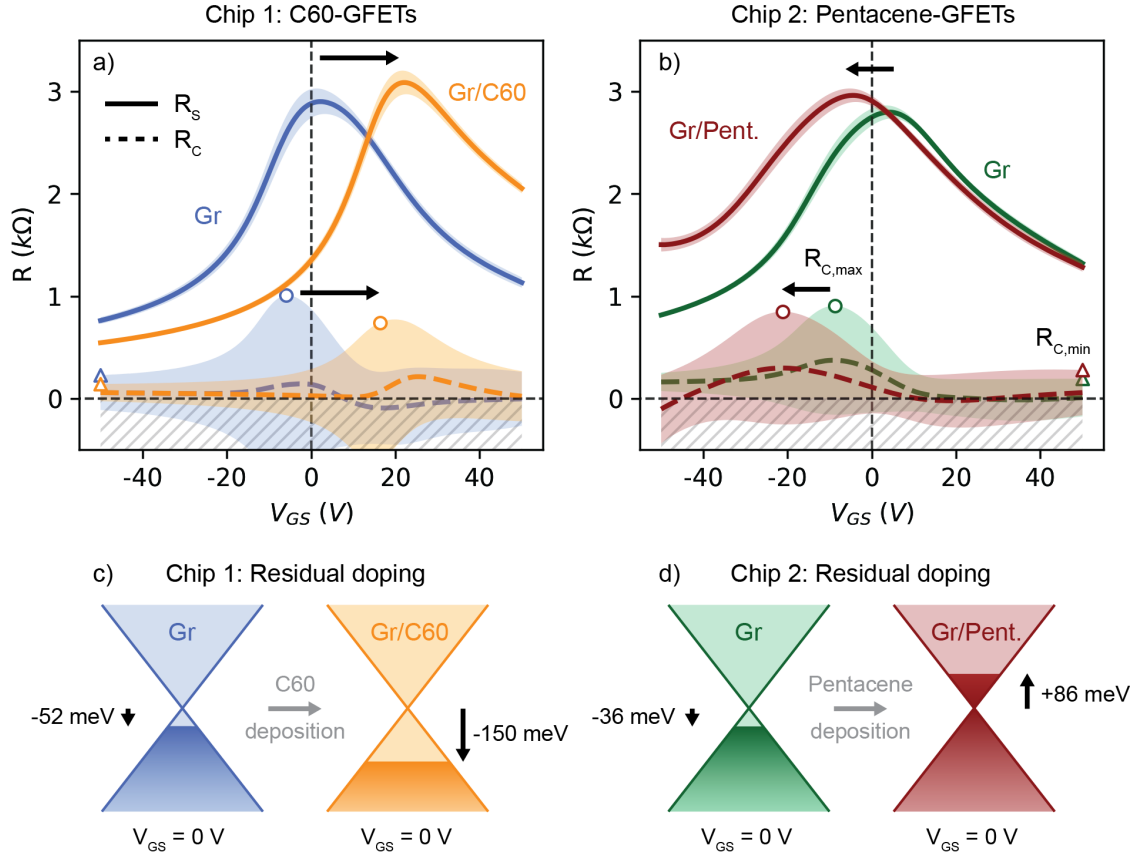
Figure 14: GFETs sheet resistance (R_S) and contact resistance (R_C) represented by solid and dashed lines, respectively. (a) R_S (solid line) and R_C (dashed line) of pristine CVD graphene before (blue) and after (orange) deposition of C60 (Chip 1). (b) R_S (solid line) and R_C (dashed line) of pristine CVD graphene before (green) and after (red) deposition of Pentacene (Chip 2). The shaded areas are the standard errors of the estimated slope and intercept of the linear regression method used to extrapolate R_S and R_C in the Transfer Length Method (TLM) from the data sets presented in Figures 13a-d. (c) Schematic of the residual p-doping of graphene due to C60 deposition (Chip 1). (d) Schematic of the residual n-doping of graphene due to Pentacene deposition (Chip 2).

Figure 14a-b show the GFETs sheet resistance (R_S) and contact resistance (R_C)

extrapolated from the transfer characteristic of Figures 13a-d using the Transfer Length Method (TLM), where the total resistance is $R_T = 2R_C + R_S l/w$, as described in the Experimental Method and in the Supporting information (Figure 39). The negative average R_C values from the uncertainty of the linear regression are discarded (hatched area). On the one hand, the sheet and contact resistances of the two sets of pristine GFETs (Figures 14a-b) showed similar characteristics: (i) they both depended on V_{GS}; (ii) the maximum of the sheet resistances, which was approximately $3\,\mathrm{k\Omega}$, was found in proximity of the Dirac point V_{GS}^{Dirac}; and (iii) the maximum of R_C, approximately $1\,\mathrm{k\Omega}$, was found for $V_{GS} < V_{GS}^{Dirac}$. The latter suggested that the hole and electron energy barrier heights at the Au / Gr interface, which results from the charge transfer between the metal electrodes and graphene,[122,123] were different.[122] On the other hand, after the deposition of the molecules: (i) the electrostatic doping reduced the sheet resistance of graphene, which approached approximately $1\,\mathrm{k\Omega}$ at $V_{GS} = \pm 50\,\mathrm{V}$; (ii) the maximum of R_S increased by approximately $200\,\Omega$ and shifted to more positive V_{GS} for the C60-GFETs and to more negative V_{GS} for the Pentacene-GFETs, possibly due to an increased charge-impurity scattering resulting in a reduced charge carrier mobility,[121] assuming that the graphene charge carrier density at V_{GS}^{Dirac} was not affected by the molecules; (iii) the maximum of R_C shifted with R_S and remained close to the Dirac point, suggesting that the charge carrier injection mechanism at the Au / Gr interface was not significantly affected by the molecules. Assuming that the charge injection mostly occured at the edge between the metal electrodes and Gr ($W = 5\,\mathrm{\mu m}$), the gate dependent contact resistivity $\rho_C = R_C W$ could be calculated and spans the range $0.5 - 5\,\mathrm{k\Omega\,\mu m}$. Table 1 summarizes all the electrical properties of the GFETs. It is worth observing, that taking into account the graphene Fermi energy shift induced by the OSCs, and using the reported HOMO and LUMO energy level of C60 and Pentacene,[1] the nominal the energy barriers at $V_{GS} = 0\,\mathrm{V}$ for electrons ($\Phi_{B0,e} = E_{LUMO} - E_{F,Gr}$) at the Gr / C60 and for holes ($\Phi_{B0,h} = E_{F,Gr} - E_{HOMO}$) at the Gr / Pentacene interfaces, resulted in about $0.6\,\mathrm{eV}$, which is within $\pm 0.1\,\mathrm{eV}$ of previously reported values obtained from the thermionic emission model.[22,55] This support the hypothesis that all interfacial phenomena at the C60/graphene and Pentacene/graphene interfaces account for only 15% of the nominal energy barriers that can be estimated from the energy diagram of the isolated molecules. These Schottky-like interfaces are favorable for the realization of graphene-based vertical organic transistors which exploit complementary n- and p-type organic semiconductors.[24,51,52,55,96,97]

Property (Unit)	Chip 1: C60-GFETs		Chip 2: Pentacene-GFETs	
	Gr	Gr/C60	Gr	Gr/Pentacene
V_{GS}^{Dirac} (V)	2.8 ± 9.1	23 ± 5.0	1.3 ± 6.7	-7.6 ± 7.5
μ_e (cm^{-2}V^{-1}s^{-1})	1430 ± 354	713 ± 261	1101 ± 227	922 ± 226
μ_h (cm^{-2}V^{-1}s^{-1})	2298 ± 399	2389 ± 333	1910 ± 310	1268 ± 275
n_0 (1×10^{12} cm^{-2})	0.20 ± 0.65	1.65 ± 0.36	0.09 ± 0.48	0.55 ± 0.54
ΔE (meV)	-52 ± 55	-150 ± 15	-36 ± 53	$+86 \pm 35$
R_S (kΩ)	0.76 ± 2.90	0.54 ± 3.09	0.82 ± 2.80	1.28 ± 2.96
R_C (kΩ)	0.23 ± 1.01	0.14 ± 0.74	0.19 ± 0.91	0.28 ± 0.85
ρ_C (k$\Omega\,\mu$m)	1.15 ± 5.05	0.70 ± 3.70	0.95 ± 4.55	1.40 ± 4.25

Table 1: Summary of the electrical properties of the GFETs before and after deposition of the C60 and Pentacene molecules. The table shows the mean and variance of the normal distributions of V_{GS}^{Dirac}, μ_e and μ_h in Figure 13e-j. The residual doping of graphene is calculated considering the mean and variance values of V_{GS}^{Dirac} in Eq. 2 before and after deposition of the molecules. The Fermi energy shift ΔE is calculated using the energy dispersion relation of graphene and residual doping. The table shows the minimum and maximum values of the gate dependent sheet resistance (R_S) and contact resistance (R_C) presented in Figure 14. The contact resistivity $\rho_C = R_C W$ is calculated using the channel width $W = 5\,\mu$m.

4.3   Conclusion

In summary, CVD Graphene Field Effect Transistors (GFETs) with a fixed channel width (5 µm) and different channel lengths (5, 10, 20, 50 and 100 µm) were fabricated and electrically characterized under vacuum. Subsequently, thin films of C60 and Pentacene were deposited on two distinct GFET chips by thermal evaporation and electrically characterized again under vacuum. The GFETs transfer characteristic revealed that the deposition of C60 on graphene results in an increased residual graphene hole-density of $(1.65 \pm 0.36) \times 10^{12}\,\mathrm{cm}^{-2}$, whereas the deposition of Pentacene results in an increased residual graphene electron-density of $(0.55 \pm 0.54) \times 10^{12}\,\mathrm{cm}^{-2}$. In both cases, the increase of the residual charge carriers is accompanied by a reduced charge mobility, possibly due to an increased charge-impurity scattering in graphene. The Fermi energy of graphene shifted to $(-150 \pm 15)\,\mathrm{meV}$ after the deposition of C60, and it shifted to $(86 \pm 35)\,\mathrm{meV}$ after the deposition of Pentacene, while the charge carrier injection at the Au/Gr did not seems to be significantly affected. Overall, this work provide useful insight on the graphene in-plane charge transport and on the energetic of the Gr / C60 and Gr / Pentacene hybrid heterostructures which could be exploited in more complex organic electronic devices. For instance, the energy barriers forming at the Gr / C60 and Gr / Pentacene interfaces and the weak electrostatic screening of graphene could be beneficial to form n- and p-type channels in graphene-based vertical organic transistors.

4.4 Experimental Methods

Chemical Vapor Deposition (CVD) of graphene

Graphene was grown in-house by Chemical Vapour Deposition (CVD) on copper foils (Thermoscientific, 25 µm thick, annealed, uncoated, 99.8%) with a fully automated setup. The foils are ultrasonicated in Acetone, rinsed with Isopropyl Alcohol (IPA) and dried with N_2. Then, the foils are placed in Acetic Acid (CH_3COOH) for 30 min, rinsed in de-ionized water (DIW) and Ethanol, and dried with N_2. The cleaned foils are pre-annealed at 1000 °C for 1 h in a H_2 (20 sccm) and Ar (200 sccm) atmosphere in the CVD oven (ca. 1 mbar). Then, graphene grows for 35 min in a CH_4 (0.05 sccm), H_2 (20 sccm) and Ar (200 sccm) atmosphere under a pressure of ca. 120 mbar. After the CH4 flow is stopped, the CVD oven is left to cool down to room temperature (at ca. 1 mbar).

Wet transfer method of CVD graphene

The CVD graphene was transferred as previously reported.[82,83] To protect graphene, a film of PMMA (50k) was spin-coated on the top side of CVD graphene/Cu foils. Then, the graphene grown on the Cu back side was removed using Reactive ion etching (RIE) in an Ar (15 sccm) and O_2 flow (30 sccm) for 2 min. The Cu substrate was etched away in a Ferric Chloride ($FeCl_3$, Transene CE-100) bath for 1 h, and then transferred to de-ionized water (DIW). Subsequently, the remaining graphene/PMMA sheet was placed in Hydrochloric acid (HCl 10%) for 5 min and transferred back to DIW. Finally, graphene could be transferred on the target substrate and dried overnight in a vacuum oven (ca. 1 mbar, 80 °C).

Graphene Field Effect Transistors (GFETs) fabrication

Two chips including 150 Graphene Field Effect Transistors (GFETs) were fabricated. Graphene sheets grown by CVD on Cu foils were transferred onto photolithography pre-patterned Ti(5 nm)/Au(50 nm) electrodes on Si(525 µm)/SiO_2(300 nm) substrates. The Au bottom contacts architecture (Figure 11) was chosen to minimize the number of lithography steps after the transfer of graphene. A double layer of PMMA 50K/950K (AR-P 632-06 / AR-P 672.02) was spin-coated on graphene, exposed to e-beam and developed for 1 min in MIBK:IPA (1:2). Then, the samples were rinsed in IPA and dried with N_2. Finally, the unprotected graphene was etched away using RIE for 30 s (15 sccm Ar, 30 sccm O_2). The remaining PMMA, protecting the graphene channels, was removed in Acetone (55 °C) for 1 h and IPA (55 °C) for 1 h.

Thermal evaporation of C60 and Pentacene

Fullerene-C60 (99.9%, sublimed) powder was purchased from Sigma-Aldrich, while Pentacene powder (99.999%, purified by sublimation) was purchased from Tokyo Chemical Industry (TCI). The two types of molecules were thermally evaporated under vacuum (ca. 1×10^{-6} mbar) without further treatments. The C60 thin film was deposited by thermal evaporation at ca. $0.2 \, \text{Ås}^{-1}$ from a Molybdenum evaporation boat (Umicore). The Pentacene thin film was thermally evaporated at ca. $0.05 \, \text{Ås}^{-1}$ using a low temperature controlled source (ca. 120 °C) with an Al_2O_3 crucible (Creaphys). The temperature of the target substrate wat not actively controlled during the evaporation.

Electrical characterization

The devices were electrically characterized under vacuum (ca. 1×10^{-6} mbar) and at room temperature. Samples were shortly exposed to ambient conditions during the transport from the evaporation chamber to the electrical prober vacuum chamber. They were kept in vacuum conditions (ca. 1×10^{-6} mbar) for at least 24 h before being characterized. The electronics comprised an AdWin Gold II ADC-DAC unit, a low-noise current to voltage converter (Femto DDPCA-300) to measure the drain-to-source current (I_{DS}) and a high-voltage amplifier (Basel SP908) to provide the gate-to-source voltage (V_{GS}). The drain-to-source voltage (V_{DS}) was directly provided by the ADC-DAC. The automated probe station and the ADC-DAC were controlled via LabVIEW and Matlab scripts. In the drain-to-source voltage (V_{DS}) sweep from -50 mV to +50 mV, the voltage step was set to 0.5 mV, the sweep rate to 50 mV/s and the gate-to-source voltage was set to 0 V. In the gate-to-source voltage (V_{GS}) sweep from -50 V to +50 V, the voltage step was set to 0.1 V, the sweep rate to 10 V/s and the drain-to-source voltage (V_{DS}) was set to 50 mV. The internal averaging was set to 20 ms for all the measurements. Only the backward sweep traces were considered for the analysis, refer to the Supporting information for the full sweeps (Fig. 36). The gate-to-source current (Fig. 37) was measured using a Semiconductor Parameter Analyzer Keithley 4200.

Atomic Force Microscopy (AFM)

The height images were measured under ambient conditions using a Bruker Icon AFM in tapping mode. The AFM was equipped with a TESPA-V2 cantilever with a tip apex radius of 7 nm, with a resonant frequency 320 kHz and a spring constant of 37 N/m. The AFM data was processed with Gwyddion which was used to extract

the single and average height profiles and export the images.

Raman spetroscopy

Raman spectra were acquired in ambient conditions using a 532 nm excitation wavelength with a WITec Alpha 300R confocal Raman microscope mounting a LD 100x objective (Zeiss EC Epiplan-Neofluar Dic, NA = 0.75) and a 300 mm lens-based spectrometer (grating: 600 g mm-1) equipped with a TE-cooled charge-coupled device (Andor Newton). One Raman spectrum for each device was collected (150 devices per chip). The laser power was set to 0.1 mW and 0.5 mW for the Gr/C60 and Gr/Pentacene heterostructures, respectively. In both cases, the integration time was set to 30 s. The average Raman spectrum of graphene, Gr/C60 and Gr/Pentacene was obtained using all the Raman spectra acquired on each set of devices. Refer to Figures S2-3 for details on the Raman spectra processing.

Data selection and anaylsis

Python scripts were used for the data selection, analysis and visualization. Raman spectra averaging and polynomial background subtraction was done using numpy.[124] The results of the electrical measurements were organized in pandas[125] dataframes. The devices showing non-linear output characteristic, low $I_{DS} \ll 1\,nA$ (open circuit) and/or more than one minima in the transfer characteristic were discarded from the analysis. Only the backward sweep of the transfer characteristics were considered for the determination of the Dirac point, the mobility and the resistances. The GFETs electron and hole mobility were extrapolated using Eq. 3 and taking the maxima of transconductance in the V_{GS} range –50 to +50 V. A Savitzky-Golay filter with window size 20 and smoothing order 3 was applied to the transfer characteristics before computing the numerical derivative dI_{DS}/dV_{GS}. A Transfer Length Method (TLM), i.e. $R_T = 2R_C + R_S$, was implemented using scipy.[126] R_C and R_S were obtained from the intercept and slope of the weighted linear regression of R_T vs. L. The weights were set to $1/R_T$. Refer to the Supporting Information for details on the Raman spectra processing (Figs. 33 and 34), the numerical derivative (Fig. 38) of the drain-to-source current (dI_{DS}/dV_{GS} and for the gate voltage dependent TLM (Fig. 39).

5 Complementary Inverter Based on C60 and Pentacene Doped CVD Graphene Field Effect Transistors on SiO$_2$

Jacopo Oswald,[a,b] Davide Beretta,[a] Michael Stiefel,[a] Roman Furrer,[a] Dominique Vuillaume,[d] Michel Calame[a,b,c]. Complementary Inverter Based on C60 and Pentacene Doped CVD Graphene Field Effect Transistors on SiO$_2$. *IEEE, Nanotechnology Materials and Devices Conference (NMDC) 2023*.

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Author contributions

Abstract

The rapid expansion of the Internet of Things (IoT) has fueled the exploration of novel materials and device architectures to meet the demands of applications such as smart wearables, environmental sensors, and flexible displays. In this context, graphene has emerged as a remarkable candidate due to its exceptional electronic and mechanical properties that are suitable for the development of flexible electronic devices. This work investigates the potential of C60- and Pentacene-doped Graphene Field Effect Transistors (GFETs) as building blocks for complementary inverters in digital and/or analog flexible electronic circuits. The fabricated complementary inverters use doped graphene as the channel material for both the n- and the p-type transistors. The channel length of the GFETs spans the range from $5\,\mu m$ to $100\,\mu m$ and does not affect the measured transfer characteristic of the inverters, which is obtained by operating the transistors between their respective Dirac points. While the GFET-based inverters show a voltage gain of about 2×10^{-2} and a bandwidth up to $10\,kHz$, circuit simulations indicate that by integrating the GFETs and by carefully designing the chip metal interconnects, the inverter could reach operating frequencies in the GHz regime. Additionally, scaling the graphene channel length allows to tune the cut-off frequency and static power dissipation of the inverter, potentially meeting the requirements of specific applications.

5.1   Introduction

Graphene-based devices have attracted significant attention due to their high mobility, flexibility and ability to conform to various surfaces.[127] The recent advancements in both the growth of large area graphene using Chemical Vapour Deposition (CVD) and the techniques for transferring graphene onto a wide variety of substrates have paved the way for the development of flexible graphene-based electronic devices,[128] which overcome some inherent limitations of traditional Silicon-based electronics. Further research on graphene-based digital and/or analog circuits is still needed to enable communications and data processing functions, and thus, to fully exploit graphene's potential for applications in smart wearables, environmental sensors and flexible displays.[129,130] In this context, different methods to induce n- and p-type behavior in Graphene Field Effect Transistors (GFETs) have been developed[77,85,131] and implemented to fabricate electronic components such as the graphene complementary inverter, which is a fundamental building block for digital circuits that produces an output signal that is the complement of its input signal.[43,44] Here, the exceptional charge carrier mobility in graphene is attractive for electronic devices requiring high frequency operation on flexible and/or transparent substrates. In addition, the techniques used for the lithography of graphene and for the deposition of organic thin films are compatible with existing electronic manufacturing workflows, making the integration of the graphene-based inverters possible and cost-effective.

In this work, we show that n- and p-type Graphene Field Effect Transistors (GFETs), obtained by doping CVD graphene with thin films of C60 and Pentacene,[85] can be assembled into working complemenatary inverters. The inverters were assembled with pairs of GFETs with fixed channel width $W = 5\,\mu m$ and length $L = 5$, 10, 20, 50, 100 μm, which were fabricated on separate chips. The output and transfer characteristics of the inverters were measured by operating the graphene transistors between their Dirac points under vacuum ($1 \times 10^{-6}\,mbar$) at room temperature (293 K). The inverter voltage gain (2×10^{-2}) and static power dissipation as a function of the graphene channels lengths were extrapolated from the current vs voltage (IV) measurements, while the dynamic response was obtained by applying digital signals (up to 10 kHz) to the devices input. The circuit simulations indicate that the fabrication of functional inverters, operating in the GHz frequency regime, should be possible by integrating the GFETs, reducing the dielectric thickness, and optimizing the metal interconnects.

5.2   Results and Discussion
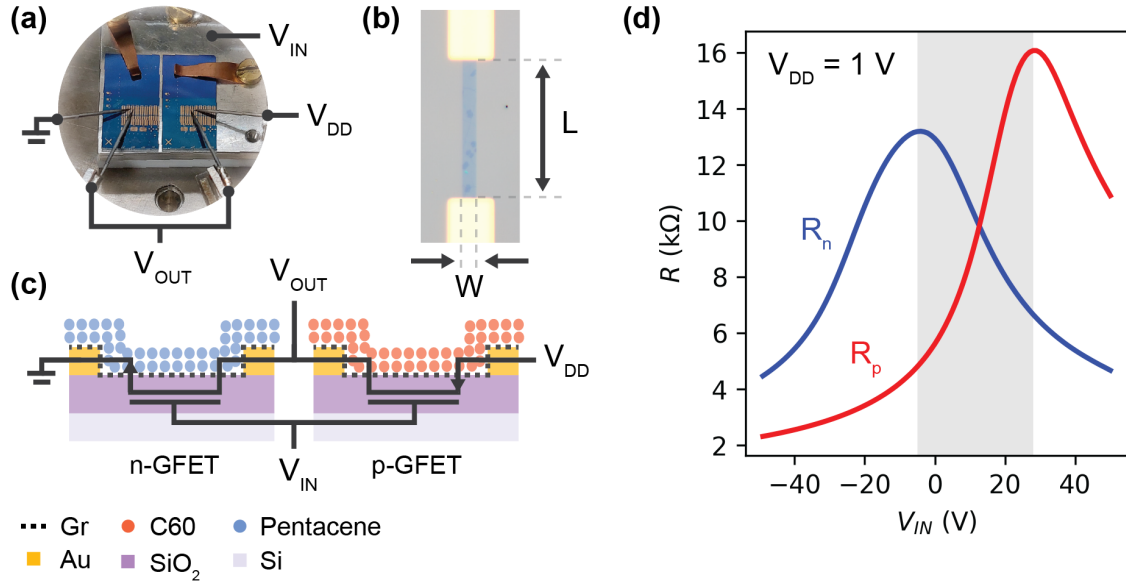
Figure 15: (a) Photograph of the n- (left) and p-doped (right) Graphene Field Effect Transistor (GFET) chips assembled into one complementary inverter. The metallic support holds the chips steady and supplies the back-gate voltage V_{IN}. The power supply V_{DD} is connected to the p-type GFET drain electrode while the source electrode of the n-type GFET is connected to ground. The inner source and drain electrodes are connected together to form the output voltage V_{OUT}. (b) Optical microscope image of a representative GFET. The channel length L and width W of this device are 50 μm and 5 μm, respectively. (c) Electrical schematic of the assembled complementary inverter (not to scale). The cross-section shows the heavily p-doped Si Gate (G), the SiO$_2$ dielectric (300 nm), the Ti/Au source/drain (5 nm/50 nm) and the p- and n-type Gr channels coated with thin films of C60 and Pentacene molecules, respectively. (d) Resistance R vs. input voltage V_{IN} measured on a representative complementary inverter assembled with two GFETs with $L = 20$ μm. R_n (blue) and R_p (red) are the resistances of the n- (left) and p-doped (right) GFETs, respectively. Complementary behavior is shown by the grey shaded area between the Dirac points of the two transistors. The Dirac points of R_n and R_p are approximately -5 V and 28 V, respectively.

Fig. 15a shows the complementary inverter assembled with pairs of n- and p-type Graphene Field Effect Transistor (GFET) fabricated on separate chips. The electrical probes were used to (i) supply $V_{DD} = 1$ V to the source electrode of the p-type GFET, (ii) connect the source electrode of the n-type GFET to ground, and (iii) join the drain electrodes of the two GFETs and measure the output voltage V_{OUT},

in formula,

$$V_{OUT} = R_n I = \frac{V_{DD}}{1 + \frac{R_p}{R_n}} \tag{4}$$

where $R_{n,p}(V_{IN})$ are the resistances of the n- and p-type graphene channels, respectively. The input voltage V_{IN} was provided by the metallic support which is in direct contact with the heavily p-doped Si substrate. Fig. 15b shows an optical microscope image of a representative GFET with graphene channel dimensions $L = 50\,\mu$m and $W = 5\,\mu$m. The CVD graphene was transferred on top of the lateral Ti/Au electrodes and subsequently patterned by ebeam lithography. Fig. 15c shows the electrical schematic and cross-section of two GFETs used to assemble a complementary inverter. The n- and p-type GFETs were obtained by thermal evaporation of thin films of Pentacene (blue circles) and C60 (red circles) on graphene (dashed black line), as previously reported.[85] Fig. 15d shows the transfer resistances $R_n = V_{OUT}/I$ in blue, and $R_p = (V_{DD} - V_{OUT})/I$ in red, as a function of the input voltage V_{IN}, for a fixed V_{DD} voltage of 1 V. The Dirac points of the n- and p-doped graphene were found at approximately -5 V and 28 V. We note that the two GFETs operate as a complementary inverter in the grey shaded region between the Dirac points. In this region, the C60 and Pentacene doped GFETs show p- and n-type behavior, respectively. Their resistances at the respective Dirac points are $R_n \approx 13\,\text{k}\Omega$ and $R_p \approx 16\,\text{k}\Omega$ and the resistances ratio is $R_p/R_n \approx 0.4$ at -5 V, while it is $R_p/R_n \approx 2.4$ at 28 V. Therefore, based on Eq. 4, the output voltage swing of the inverter should be limited to ca. $0.3 - 0.7$ V. The field-effect mobility:

$$\mu = \frac{L g_m}{W C_{GS} V_{DS}} \tag{5}$$

was extrapolated using the maximum of the transconductance $g_m = max(dI_{DS}/dV_{GS})$.[85] The electron and hole mobilities were approximately $\mu_e \approx 1000$ cm^{2}V^{-1}s^{-1} and $\mu_h \approx 2000$ cm^{2}V^{-1}s^{-1} for the n-type and p-type transistors, respectively. This relatively high carrier mobility, combined with the mechanical properties of graphene, is attractive for applications requiring high speed operation on flexible substrates.
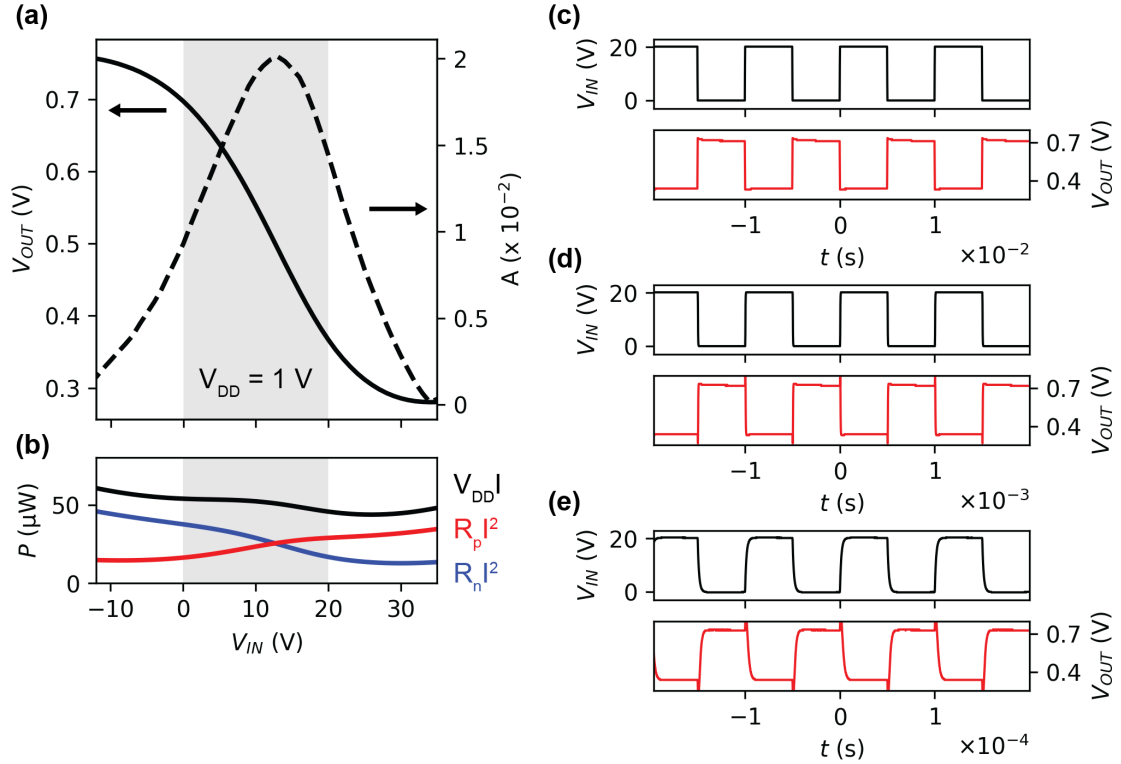
Figure 16: (a) Output voltage V$_{OUT}$ (solid line) and voltage gain A (dashed line) vs. input voltage V$_{IN}$ of a representative complementary inverter assembled with two GFETs with $L = 20\,\mu$m. (b) The static power dissipation of the inverter (black) and the power dissipated by the transistors through R$_p$ (red) and R$_n$ (blue). The dynamic response of the inverter is obtained by applying digital signals with low and high logic levels of $0\,$V and $20\,$V (grey dashed area). (c-e) Dynamic response of the the complementary inverter assembled with two representative GFETs with L = 20 μm and for $V_{DD} = 1$ V. The input signal V_{IN} (black) frequency is: (c) $f = 100\,$Hz, (d) $f = 1\,$kHz, and (e) $f = 10\,$kHz. The output voltage V_{OUT} is shown in red.

Fig. 16a shows the output voltage V_{OUT} as a function of the input voltage V_{IN} (solid line) of the inverter with $L = 20\,\mu$m for both GFETs channels, for a fixed $V_{DD} = 1$ V. The voltage gain $A = |dV_{OUT}/dV_{IN}|$ is indicated by the dashed line. The device shows the characteristics of an inverter with a measured output voltage swing of about $0.28 - 0.75$ V and a maximum voltage gain of 2×10^{-2}. It is worth noticing that an inverter with a voltage gain lower than unity is not functional for applications because it attenuates the input signal instead of amplifying it, resulting in a weaker output. Furthermore, it cannot be cascaded with other inverters since each stage would further reduce the voltage magnitude, leading to cumulative signal attenuation and rendering the cascaded system unusable. A voltage gain greater than unity could be achieved by optimizing the GFETs gate dielectrics and increasing

the supply voltage V_{DD},[44] resulting however in an increase of the power dissipation. Fig. 16b shows the static power dissipation ($P = V_{DD}I$) of the inverter in black, the power dissipated by R_p in red and the power dissipated by R_n in blue. The static power dissipation of the inverter, which is the sum of the power dissipated by R_n and R_p ($P = R_nI^2 + R_pI^2$), is about 50 µW and roughly independent from V_{IN}, and thus, the static power dissipation is substantial compared to conventional CMOS inverters. Therefore, the graphene inverters can only be employed for applications requiring high speed operation and where the power dissipation is not a concern. Figs. 16c-e show the dynamic response of the inverter to digital signals with frequencies of 100 Hz, 1 kHz and 10 kHz. The inverters characteristic shows well defined and stable output logic levels up to 10 kHz, where the signal distortion is attributed to low-pass filter of the high-voltage amplifier that was used to generate V_{IN} with a high logic level of 20 V. We note that the input voltage can be decreased by reducing the thickness of the SiO$_2$ dielectric and the voltage supply adjusted, enabling a matching of the input and output voltage levels to achieve a functional inverter.
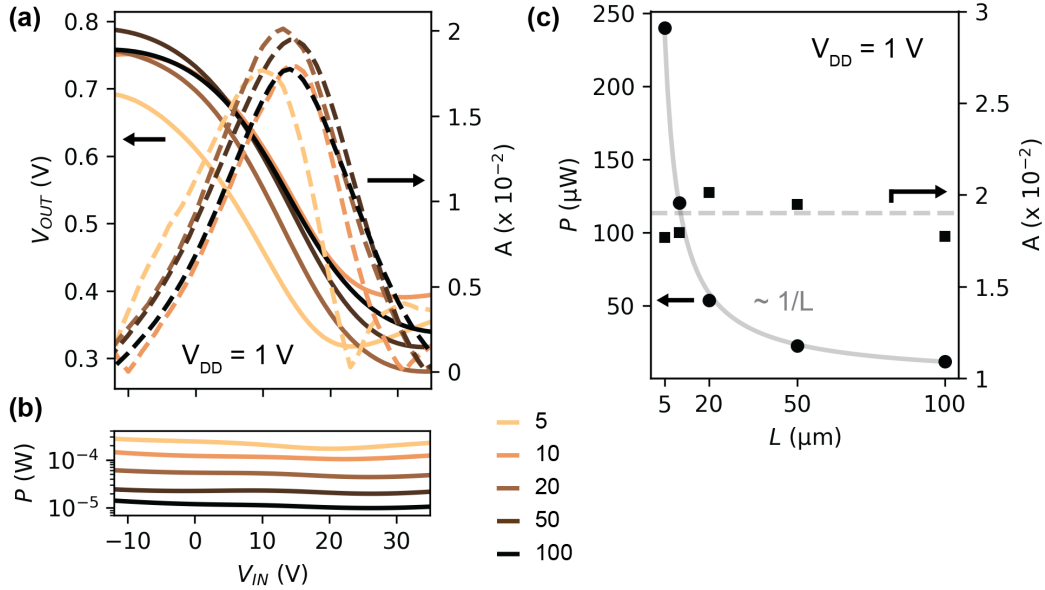
Figure 17: Transfer characteristics of the complementary inverters. (a) V_{OUT} (solid lines) and voltage gain A (dashed lines) vs. V_{IN} and (b) Static power dissipation P vs. V_{IN} of the inverters with channel length L = 5, 10, 20, 50 and 100 µm and width $W = 5$ µm. (c) Static power dissipation P (circles) and voltage gain A (squares) of the graphene complementary inverter vs. channel length L. The solid grey line shows the $1/L$ trend of the static power dissipation. The dashed grey guideline indicates the constant voltage gain. The numerical values of V_{swing}, A and P of the inverters are reported in Table 4 in Appendix C.

Fig. 17a shows the V_{OUT} vs V_{IN} characteristic of the inverters assembled with pairs of GFETs with L = 5, 10, 20, 50 and 100 μm. The corresponding voltage gains A are indicated by the dashed lines. The transfer characteristics of the different inverters display similar output voltage V_{OUT}, ranging from about 0.3 V to 0.8 V, and maximum voltage gain A of about 2×10^{-2}. Thus, the voltage swing V_{swing} and gain A are not affected by the scaling of the transistors channel length L. In contrast, the static power dissipation P ranges from about 12 µW, for the device with the longest channels ($L = 100$ µm), to about 240 µW for the shortest device ($L = 5$ µm), as shown in Fig. 17b. It is important to note that the relatively high power dissipation could limit the range of applications of the graphene-based inverters. To design devices that can meet the specific needs of applications in flexible electronics, it is crucial to find the right trade-off between power consumption and frequency response and thus, to understand how these parameters scale with the dimensions of the transistors. Fig. 17c reports the static power dissipation and voltage gain of the inverters as a function of the channel length L. We observe that static power dissipation scales as $1/L$, inversely proportional to the channel resistance ($R_{n,p} \approx L/W$), while the voltage gain A is constant and about 2×10^{-2}. Therefore, the static power dissipation of the inverter can be tuned by varying the channel resistance, without affecting the output voltage swing and voltage gain. On the other hand, an increase of the channel resistance $R_{n,p}$ correspond to a decrease of the inverter cut-off frequency. Considering the gate-oxide capacitance, i.e. $C_{ox} = \epsilon_0 \epsilon_r LW/t$, where ϵ_0 is the vacuum permittivity, while $\epsilon_r = 3.9$ and $t = 300$ nm are the dielectric constant and thickness of SiO$_2$, the cut-off frequency of the inverter is $f_c \approx 1/(2R_{n//p}C_{ox}) \approx 1/L^2$. Accordingly, the cut-off frequency of the graphene inverter shown in Fig. 17c, with $R_{n//p} \approx 4$ kΩ and $C_{ox} \approx 12$ fF, is approximately 1.8 GHz. Nevertheless, the the actual cut-off frequency of the inverters is limited by the graphene channel resistance and the system load capacitance, as shown in the following circuit analysis.

Fig. 18a shows the equivalent electrical circuit of the arbitrary signal generator connected to the high-voltage amplifier, which has a cut-off frequency of 100 kHz and an output resistance $R_{HV} = 10\,\Omega$ ($C_{HV} = 160$ nF), and of the oscilloscope channel 1, which is modeled by the parallel input resistance $R_{CH1} = 1$ MΩ and capacitance $C_{CH1} = 20$ pF. Fig. 18b shows the equivalent electrical circuit of the graphene complementary inverter, where the gate-to-source capacitance of the single GFET is calculated as $C_{GS} = C_{PAD} + C_{ox} \approx C_{PAD} = 5$ pF. Since the geometrical capacitance of the Au metal pads C_{PAD} is large (the surface is $A = 150$ µm $\times$ 150 µm), the gate-oxide capacitance can be neglected. The drain-to-source capacitance $C_{DS} = 40$ pF

was measured with the LCR meter. The resistances R_p and R_n were modeled by a polynomial of the form $R(V_{IN}) = aV_{IN}^3 + bV_{IN}^2 + cV_{IN} + d$, which coefficients were obtained by fitting the polynomial to the data shown in Fig. 40 in Appendix C. Fig. 18c shows the equivalent electrical circuit of the output measurement setup including the load capacitance C_L, which takes into account the cables and instrumentation, and the oscilloscope channel 2, which is modeled by the parallel input resistance $R_{CH2} = 1\,\text{M}\Omega$ and capacitance $C_{CH2} = 20\,\text{pF}$.
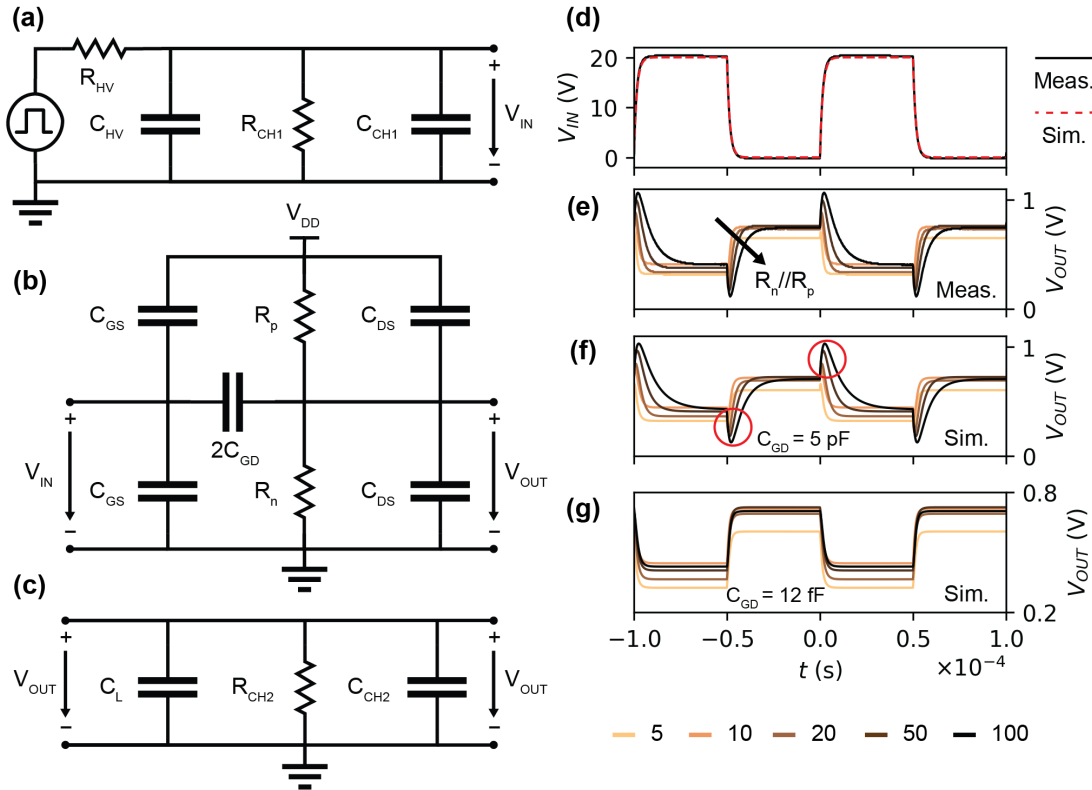
Figure 18: (a) Equivalent circuit of the digital signal generator including the 1 V square waveform generator, the 10x high-voltage amplifier with a 100 kHz low-pass filter and an output resistance $R_{HV} = 10\,\Omega$, and the oscilloscope channel 1 with $R_{CH1} = 1\,\text{M}\Omega$ and $C_{CH1} = 20\,\text{pF}$. (b) Equivalent circuit of the complementary inverter with $C_{GS} = 5\,\text{pF}$ and $C_{DS} = 40\,\text{pF}$. (c) Measured load capacitance $C_L = 250\,\text{pF}$ and the oscilloscope channel 2, with $R_{CH2} = 1\,\text{M}\Omega$ and $C_{CH2} = 20\,\text{pF}$. (d-g) Dynamic response of the inverters to digital input signal with frequency $f = 10\,\text{kHz}$. (d) Measured (solid black line) and simulated (dashed red line) input voltage V_{IN}. (e) Measured output voltage V_{OUT} of the inverters with channel length L = 5, 10, 20, 50 and 100 µm and width $W = 5\,\text{µm}$. (f) Simulated output voltage V_{OUT}. (g) Simulated output voltage V_{OUT} for an optimized circuit, where $C_{GS} = C_{GD} = C_{DS} = C_{ox} = 12\,\text{fF}$.

Fig. 18d shows the measured (solid black line) and simulated (dashed red line) input voltage. The time constant of the system is given $\tau \approx RC$, where $R \approx R_p // R_n$ and $C \approx C_L > C_{ox}$. Accordingly, increasing the length of the graphene channels leads to higher resistance R, and therefore, a slower time response, as shown in Fig. 18e. On one hand, the capacitive loading of the output, which is mostly due to the measurements instruments, can be reduced to $C \approx C_{ox}$ by integrating the devices on a single chip, and therefore, enabling an higher operational frequency. On the other hand, the capacitance of the metal interconnects C_{PAD} can be minimized by implementing a local gate. This would result in a reduction of the gate-to-drain capacitance to $C_{GD} = C_{PAD} + C_{ox} \approx C_{ox}$ and would avoid the loading curves circled in red in Fig. 18f. In fact, the circuit simulation with optimized interconnects, i.e. $C_{PAD} \approx 0\,\mathrm{F}$, no longer produces these loading curves, as shown in Fig. 18g. We note that the reduction of the dielectric thickness will not only enable the matching of the input and output voltage levels but will also increase the gate oxide capacitance, leading to a slower time response of the inverter.

5.3   Conclusion

In summary, the devices presented in this work, which were assembled using C60 and Pentacene doped GFETs, demonstrated the characteristics of complementary inverters. The results set a promising base to the subsequent fabrication of an integrated inverter. From our results, we anticipate that the fabrication of functional inverters operating in the GHz frequency regime should be possible by integrating the GFETs on a single chip, reducing the dielectric thickness, and optimizing the metal interconnects, all steps being feasible with current state-of-the art fabrication processes.

5.4 Experimental methods

Device Fabrication

The fabrication process of Graphene Field Effect Transistors (GFETs) and the deposition of C60 and Pentacene thin films are described. A more detailed description of the GFETs fabrication process, including information on the Chemical Vapor Deposition (CVD) of graphene, can be found elsewhere.[82, 85, 132] Briefly, the CVD graphene foils were wet transferred on Si/SiO$_2$ (525 µm / 300 nm) substrates with pre-patterned Ti/Au (5 nm / 50 nm) electrodes. The graphene was then patterned using e-beam lithography and Reactive ion etching (RIE) to create geometrically defined channels with lengths L = 5, 10, 20, 50, 100 µm and width $W = 5$ µm. Thin films of C60 (about 10 nm) and Pentacene (about 5 nm) were thermally evaporated onto two separate GFET chips, which were subsequently connected with electrical measurement probes to realize a complementary inverter.

Electrical Characterization

All the devices were measured under vacuum (1×10^{-6} mbar) and at room temperature (293 K). A Semiconductor Parameter Analyzer Keithley 4200 was used for the I-V characterization. The square wave signals ($0 - 2$ V) were generated using a Tektronix AFG 3102 that was connected to a high-voltage amplifier (Basel SP908) to provide the digital input voltage V_{IN} ($0 - 20$ V). The positive voltage $V_{DD} = 1$ V was supplied by a Yokogawa 7651 DC soruce. The input and output voltages were measured using a Tektronix TDS 2024C oscilloscope. The device and load capacitances were measured with a BK Precision 895 LCR meter.

Data Analysis and Circuit Simulation

Python scripts were used for the data analysis and visualization of the acquired data. Numpy[124] and Scipy[126] libraries were mainly used for the processing and fitting of the measured data. Only the continuous backward sweep of the transfer characteristics were considered for the analysis. The measurement setup and the complementary inverter circuits were simulated using LTspice 17.1.18.

6 Charge transport across Au-P3HT-Graphene Van der Waals vertical heterostructures

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Abstract

Hybrid van der Waals (vdW) heterostructures based on 2D materials and/or organic thin films are being evaluated as potential functional devices for a variety of applications. In this context, the Graphene/Organic Semiconductor (Gr / OSC) heterostructure could represent the core element to build future vertical organic transistors based on two back-to-back Gr / OSC diodes sharing a common graphene sheet, which functions as base electrode. However, the assessment of the Gr / OSC potential still requires a deeper understanding of the charge carrier transport across the interface as well as the development of wafer-scale fabrication methods. This work investigates the charge injection and transport across Au / OSC / Gr vertical heterostructures, focusing on poly(3-hexylthiophene-2,5-diyl) (P3HT) as OSC, where the PMMA-free graphene layer functions as top electrode. The structures are fabricated using a combination of processes widely exploited in semiconductor manufacturing and therefore are suited for industrial upscaling. Temperature dependent current-voltage measurements and impedance spectroscopy show that the charge transport across both device interfaces is injection-limited by thermionic emission at high bias, while it is space charge limited at low bias, and that the P3HT can be assumed fully depleted in the high bias regime. From the space charge limited model, the out-of-plane charge carrier mobility in P3HT is found equal to $\mu \approx 2.8 \times 10^{-4} \, \mathrm{cm^2/Vs}$, similar to the in-plane mobility reported in previous works, while the charge carrier density results in $N_0 \approx 1.16 \times 10^{15} \, \mathrm{cm^3}$, also in agreement with previously reported values. From the thermionic emission model, the energy barriers at the Gr / P3HT and Au / P3HT interfaces result in $0.30 \, \mathrm{eV}$ and $0.25 \, \mathrm{eV}$, respectively. Based on the measured barriers heights, the energy band diagram of the vertical heterostructure is proposed under hypothesis that P3HT is fully depleted.

6.1 Introduction

Hybrid van der Waals based on 2D materials and/or organic thin films are being extensively studied[2–4] for a variety of applications encompassing field effect transistors, organic solar cells,[133–135] photodetectors,[90,136] vertical transistors[24,51,52,95] and light emitting diodes.[137,138] Despite solid progress, developing a better understanding of the electron transport across hybrid van der Waals interfaces remains crucial to better control functionality and enhance performance. In this context, graphene is an excellent candidate as 2D electrode to contact organic thin films due to its inherent ability to form $\pi - \pi$ stacking and van der Waals bonds.[139] Many studies to date aimed at unraveling the physical mechanisms behind charge injection at Gr / OSC interfaces for applications in diverse fields of micro- and nano-electronics:[1,5,140] typically, graphene is used as bottom electrode in barristors,[24,51,52,55,95,97] or transferred on top of an OSC film together with a protecting polymer, e.g. PMMA. However, other more complex multi-layer designs could benefit from graphene full potential as monoatomic thick, semi-transparent, flexible and surface-conformal electrode. For instance, graphene could replace the base in vertical transistors, enabling organic transistors with nanoscale channels and higher operation frequencies that could meet the requirements of high-frequency applications, or function as inter-layer electrode in OLEDs.[61,63,70,75] In this framework, the development of large-scale photolithographic fabrication methods compatible with hybrid architectures that exploit graphene as top or inter-layer electrode, and the understanding and modeling of the charge transport in the latter is crucial for the design and optimization of novel functional devices.

For this study, the authors developed a fabrication process for Au / Gr / P3HT hybrid vdW heterostructures, where PMMA-free graphene lies on top of a p-type OSC and functions as top electrode for the vertical stack, and investigated and modeled the charge injection across the two interfaces, i.e. Au / P3HT and P3HT / Gr, by temperature-dependent I-V measurements, impedance spectroscopy and Kelvin Probe Force Microscopy (KPFM). The charge transport across the device was found to be described by the termionic emission (TE) assisted by image-charge induced barrier lowering model in the high voltage regime ($|V| > 1\,\mathrm{V}$) and by the Space-Charge Limited (SCL) current model in the low voltage regime ($|V| < 1\,\mathrm{V}$). The models allowed to extract the charge carrier concentration and the out-of-plane mobility of P3HT, and the reduced effective Richardson constant of- and the potential barriers height at- the two interfaces, ultimately making possible to sketch the energy band diagram of the whole stack.

6.2   Experimental Methods

Materials

Poly(3-hexylthiophene-2,5-diyl) (regio-regular (RR) > 99%, Mn = 27'000 − 45'000) was purchased from Tokyo Chemicals and used as received to prepare solutions of $10 \, mg \, mL^{-1}$ in chlorobenzene. Graphene was grown in-house by Chemical Vapour Deposition (CVD) on copper foils with a fully automated setup. The graphene growth protocol can be found in previously reported works.[83,141,142]

Fabrication

The study was conducted on a single chip including two different sets of devices: (i) Au / P3HT / Gr vertical stacks (119 devices) and (ii) graphene bridges (34 devices) (refer to Fig. 19a and 20a for a schematic of the devices architecture). The chip was fabricated on a Si (525 μm) / SiO$_2$ (300 nm) substrate at the Binnig and Rohrer Nanotechnology Center (BRNC) and Empa. In both architectures, P3HT is sandwiched between a gold (bottom) and a graphene (top) circular electrode. In the bridge architecture, graphene is side-contacted so that one can force a current through it to evaluate its resistance independently from the underlying P3HT film (see Figure 2a for the electrical scheme). The chip includes devices having various nominal diameter, i.e. 5, 10, 15, 20, 25, 30 and 50 μm. The bottom gold electrodes are 2 μm larger than the top graphene electrodes. The fabrication was done by photolithography under ambient conditions as illustrated in Figure 19b and thoroughly described in the supporting information. Briefly, Au electrodes were deposited by e-beam physical vapour deposition (EBPVD) and patterned by lift-off. Then, P3HT was spin-coated at 1000 rpm for 60 s and patterned by lift-off. Finally, the CVD graphene top electrode was wet transferred and patterned by Reactive ion etching (RIE).

Electrical characterization

The electrical characterization at room temperature was done in dark, in air, under vacuum ($\approx 1 \times 10^{-6}$ mbar), using a Keithley 236 Source-Measure unit controlled via Python. The voltage was swept in the range from -10 V to 10 V in steps of 50 mV, with sweep rate of ca. $100 \, mV \, s^{-1}$ and internal averaging of 20 ms, keeping the bottom Au electrode on ground. The graphene resistance was characterized in graphene bridge devices by sweeping the voltage in the range from -50 mV to 50 mV in steps of 1 mV, with sweep rate of ca. $3 \, mV \, s^{-1}$ and internal averaging of 20 ms. The temperature-dependent I-V traces were collected in the range 200 K to 300 K

in steps of $5\,\mathrm{K}$ in a Lakeshore probe station (CRX-6.5K) operating under vacuum ($\approx 1 \times 10^{-6}\,\mathrm{mbar}$), in dark. The electronics comprised an AdWin Gold II ADC-DAC unit operating at $100\,\mathrm{kHz}$ and a low-noise current to voltage converter (Basel SP983C). The ADC-DAC was controlled via Python. The voltage was swept in the range from $-10\,\mathrm{V}$ to $10\,\mathrm{V}$ in steps of $0.1\,\mathrm{V}$, with internal averaging of $20\,\mathrm{ms}$ and delay between source and measure of $100\,\mathrm{ms}$, corresponding to an effective voltage sweep rate of ca. $0.8\,\mathrm{V\,s^{-1}}$.

Impedance spectroscopy was carried out on one representative device per area using an Agilent 4294a Precision Impedance Analyzer controlled via Python, from $40\,\mathrm{Hz}$ to $1\,\mathrm{MHz}$ in 201 steps, in dark, under vacuum ($\approx 1 \times 10^{-6}\,\mathrm{mbar}$), with oscillator level set to $100\,\mathrm{mV}$. Open/short compensation was performed after the acquisition and following the Agilent impedance measurement handbook.[89] To this purpose, devices for the open/short compensation were designed and fabricated on the same chip.

KPFM measurements were carried out at room temperature in air ($22\,^\circ\mathrm{C}$ and 35% relative humidity) with a Dimension 3100 (Bruker), using a Pt / Ir tip. Topography (tapping mode AFM) and KPFM images were recorded using a standard two-pass procedure, in which each topography line acquired in tapping mode is followed by the acquisition of CPD (contact potential difference between the tip and the sample) data in a lift mode. Since the CPD images on Au, Gr and P3HT are acquired with the same tip, the interface barrier energy is directly given by the difference in the CPD values, i.e., $\Phi_{B,Gr/P3HT} = q(CPD_{Gr} - CPD_{P3HT})$, where q is the electron charge.

Raman spetroscopy

Raman spectra were acquired in ambient conditions using a $532\,\mathrm{nm}$ excitation wavelength with a WITec Alpha 300R confocal Raman microscope mounting a LD 100x objective (Zeiss EC Epiplan-Neofluar Dic, $NA = 0.75$) and a $300\,\mathrm{mm}$ lens-based spectrometer (grating: $600\,\mathrm{g/mm}$) equipped with a TE-cooled charge-coupled device (Andor Newton). P3HT powder and films spectra were acquired by averaging over a 5 x 5 $\mu\mathrm{m}^2$ area with a laser power and integration time of $0.1\,\mathrm{mW}$ and $0.1\,\mathrm{s}$, while graphene spectra with laser power and integration time of $1\,\mathrm{mW}$ and $10\,\mathrm{s}$.

Atomic Force Microscopy (AFM)

AFM height and phase images were collected in tapping mode in ambient conditions using a Bruker Icon AFM equipped with a TESPA-V2 cantilever with a tip apex radius of $7\,\mathrm{nm}$ (resonant frequency: $320\,\mathrm{kHz}$, spring constant $37\,\mathrm{N\,m^{-1}}$).

FIB-SEM

The device cross-section was prepared by means of a FEI Helios 660 G3 UC FIB / SEM-System. Prior to cutting a protective layer of Platinum was deposited in a two-step process, first by electron induced deposition (3 keV, 800 pA), followed by ion induced deposition (30 keV, 230 pA) in order to prevent ion induced damage to the layers of interest. The cross-section was cut in a 30 kV gallium ion beam at an ion current of 47 nA. The cross-section was sequentially polished at different ion currents, down to a minimal current of 790 pA.

Modeling, fitting and plotting

Modeling, fitting and plotting of the data were done in Python. Three main libraries were used (i) *numpy polyfit*,[124] for the estimation of graphene series resistance, (ii) *scipy curve_fit*,[126] for the SCL and TE modeling and (iii) *impedance.py*[143] for the circuit modeling and fitting of the impedance analysis measurements.

6.3 Results and Discussion
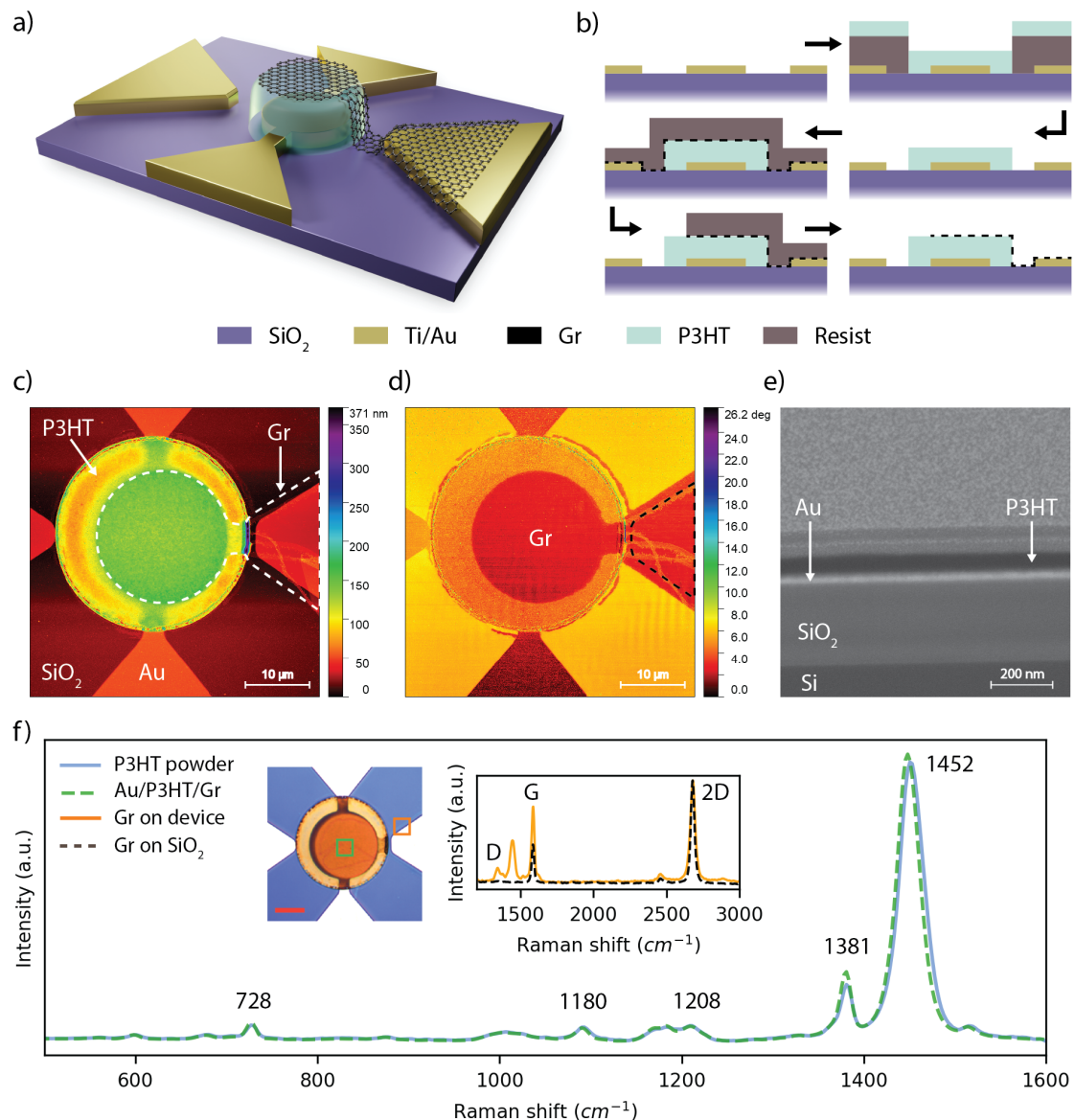
Figure 19: (a) 3D schematic of a representative Au / P3HT / Gr heterostructure (not in scale). (b) Schematic of the fabrication process. AFM (c) height and (d) phase images of a representative 20 µm device. (e) SEM of a FIB cut cross-section of a representative Au / P3HT / Gr heterostructure in the center of the device. (f) Raman spectra of P3HT powder (blue line) and of a representative Au / P3HT / Gr device (dashed green line). The optical image shows the acquisition position of the spectra (the red scale bar is 10 µm). The inset shows the Raman spectra of a device graphene against the Raman spectrum of a representative CVD graphene on SiO$_2$.

Figure 19a shows the schematic of a Au / P3HT / Gr heterostructure, fabricated according to the procedure illustrated in Figure 19b and described in the Experimental

methods and in the supporting information. Figures 19c-d show the AFM height and phase images of a representative device having a diameter of 20 μm, where a white dashed line marks the contour of the graphene and a black dashed line marks the Au side-electrode. The thickness of the Au / P3HT / Gr stack in the center of the device is ca. 130 nm as measured by AFM (see Appendix D). Given that the bottom Ti / Au electrode is 35 nm thick, the thickness of the P3HT film is ca. 100 nm. Figure 19e shows a cross-section of the Au / P3HT / Gr stack in the center of the device. Starting from the bottom, one can distinguish: Si (525 μm), SiO_2 (300 nm), Ti (5 nm), Au (30 nm) and P3HT (100 nm) as annotated in the figure. The Graphene electrode is too thin to be visible in the cross-section. Figure 19f superimpose the Raman spectrum of the P3HT powder as received, with the Raman spectrum of the Au / P3HT / Gr stack. The vibrational modes of P3HT are found at 728, 1180, 1208, 1381 and 1452 cm^{-1}, in agreement with the literature.[144,145] The vibrational modes of graphene are not discernible from P3HT for three reasons: (i) the G and D peaks of graphene are hidden by the overlapping modes of P3HT at 1381 and 1452 cm^{-1}, (ii) the 2D peak is hidden by the strong background signal of P3HT and (iii) the P3HT is much thicker than graphene, therefore resulting in a much stronger spectral signal. Therefore, the Raman spectrum of graphene was measured on SiO_2, in close proximity to the Au contact. The graphene Raman spectrum is shown in the inset of Figure 19f against the Raman spectrum of a representative CVD graphene on SiO_2. The characteristic G (1580 cm^{-1}) and 2D (2680 cm^{-1}) peaks of graphene[146] are identified, as well as the D (1350 cm^{-1}) peak, possibly due to defects induced by the fabrication, and an additional peak at 1445 cm^{-1}, most likely due to P3HT or resist residues. The AFM, SEM and Raman data demonstrate that the fabrication process is compatible with P3HT and graphene and therefore suitable for the fabrication of vertical van der Waals devices based on these materials.
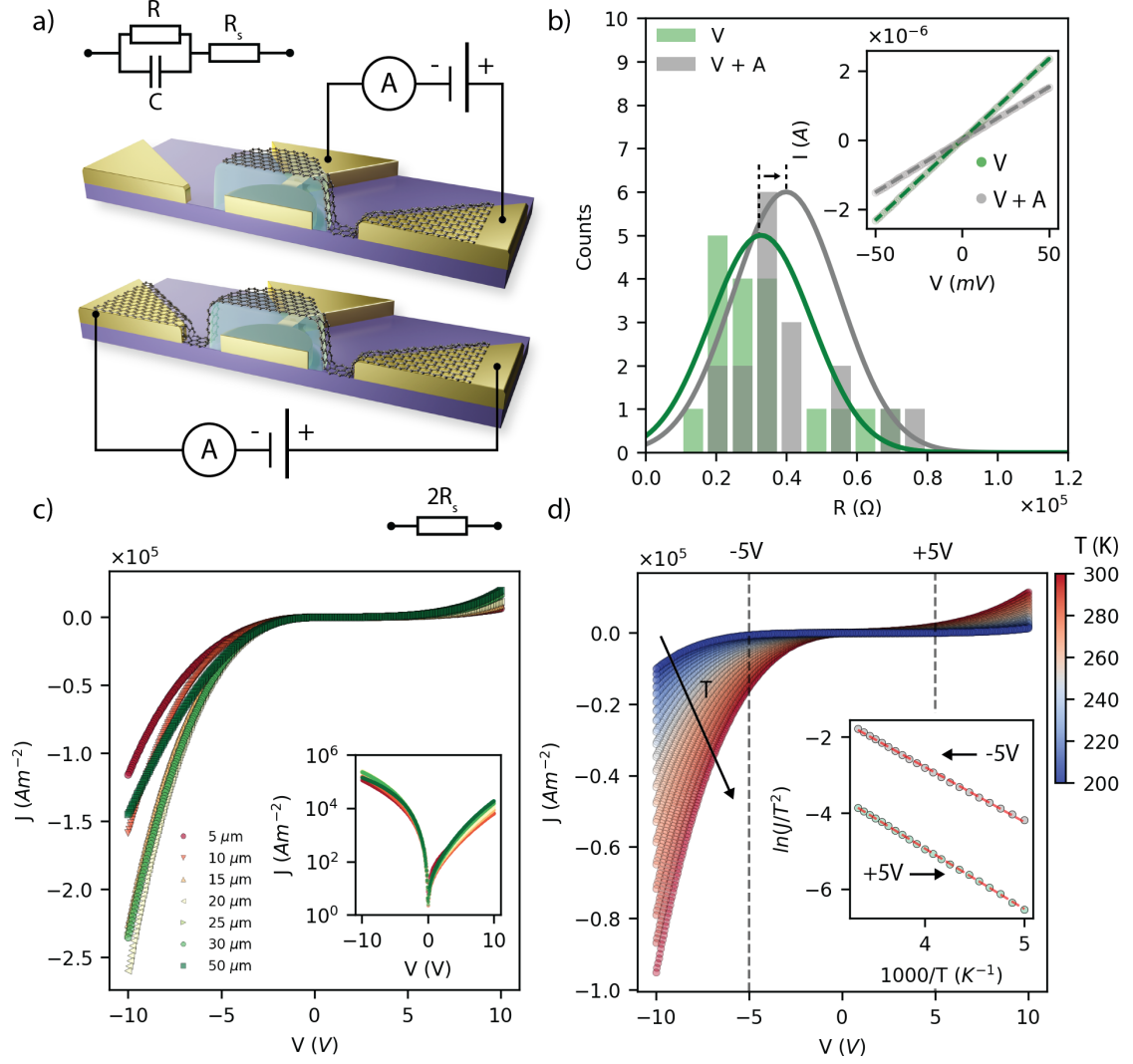
Figure 20: (a) Device schematics and electrical schemes of the Au / P3HT / Gr stack and of the graphene bridge devices. R_s is the graphene series resistance, R is the out-of-plane resistance and C is the geometrical capacitance of the device. (b) Distribution of R_s in vacuum and in vacuum after annealing (17 samples). The inset shows two representative I-V traces of side-contacted graphene. The resistance is calculated from the linear fit (dashed lines). (c) Current density of representative devices with diameter 5, 10, 15, 20, 25, 30 and 50 µm. The inset shows the same traces on log scale. (d) Temperature dependent J-V characteristic of a 5 µm device from 200 K to 300 K in steps of 5 K. The inset shows the Richardson plot for 5 V and −5 V

The electrical properties of OSCs are very sensitive to the environment. Figure 43 shows the J-V traces of a representative 10 µm device measured in ambient, in vacuum and in vacuum after annealing at 110 °C for 12 h. The current density is higher in ambient and it decreases in vacuum, reaching a minimum after annealing,

with peak current density at $-10\,\text{V}$ going from $5.4\times10^5\,\text{A/m}^2$ to $1.5\times10^5\,\text{A/m}^2$. The traces are asymmetric: defining the rectification ratio as $RR = J(-10V)/J(10V)$, the latter increases from $RR = 1.9$ in ambient, to $RR = 2.6$ in vacuum and finally $RR = 19.2$ in vacuum after annealing. This trend is ascribed to the graphene and P3HT de-doping: it is known that P3HT is doped by O_2,[147] while Graphene is doped by O_2 and H_2O,[107–109] and that their doping level can be reduced by annealing under vacuum.[148,149] Accordingly, an annealing under vacuum shifts the Fermi level of graphene, resulting in a re-alignment of the energy bands at the OSC / graphene interface, which leads to the observed change in the rectification ratio. The hypothesis is further supported by the graphene resistance shown in Figure 20b: the graphene / Au interface is Ohmic and the graphene resistance increases after vacuum exposure and annealing.

In order to minimize the variability among different devices due to uncontrolled doping of P3HT and graphene, the charge transport analysis that follows was done in vacuum after annealing for $12\,\text{h}$ at $110\,\text{°C}$. Figure 20c shows the current density of five representative devices, one per device area, measured in vacuum after annealing (see supporting information for the J-Vs of all devices). The current density is calculated assuming the area of the (smaller) graphene electrode ($J = I/A_{Gr}$). The current density variability falls within ca. one order of magnitude (between 7.3×10^4 and 2.6×10^5 at $-10\,\text{V}$, and between 3.1×10^3 and 2.3×10^4 at $10\,\text{V}$) and all J-Vs display the same shape. This suggests that the scaling of the device, from $50\,\mu\text{m}$ down to $5\,\mu\text{m}$ in diameter, does not affect the transport mechanism, and that the variability between devices is due to fabrication uncertainties. In all measurements conditions, and for both positive and negative bias, the current density grows exponentially with the applied voltage above a certain threshold. This trend is typically described by a variety of analytical models that allows to extract transport parameters (e.g. charge carrier mobility and density, and the energy barriers at the interfaces). Among these models are the termionic emission (TE) assisted by image-charge-induced potential barrier lowering,[150] the Poole-Frenkel Emission (PFE)[150] and the Modified TE (MTE) for graphene/semiconductor interfaces.[50,151] The fittings of the J-Vs with the PFE model (not reported) were found to return relative dielectric permittivity of P3HT around 20-40, i.e. about one order of magnitude larger than what discussed in the literature.[152–154] Therefore, the PFE model was excluded from the analysis. The hypothesis of the MTE model requires that the charge at the graphene / semiconductor interface depends on the bias. However, the capacitance measurements discussed in the following show that the organic semiconductor is fully depleted. Hence, the charge at the interface is bias independent

and therefore the MTE model was not considered for the analysis that follows. The TE model has been successfully applied to metal-OSC interfaces[48,155–157] and was found to be in good agreement also with the measurements of this work in the high voltage regime, that is $|V| > 1V$. According to the TE model, the J-V traces shown in Figure 20c are the reverse currents of the Au / P3HT and Gr / P3HT interfaces for negative and positive bias, respectively. The reverse current reads:[150]

$$J = A^{**}T^2 \exp\left[-\frac{q(\phi_B - \sqrt{qV/4\pi\epsilon_0\epsilon_r t})}{kT} \right] \qquad (6)$$

Where A^{**} is the reduced effective Richardson constant, T is the temperature, q is the elementary charge, Φ_B is the barrier height potential, ϵ_0 is the vacuum permittivity, ϵ_r is the P3HT dielectric permittivity, k_B is the Boltzmann constant, t the thickness of the device, and $V' = V - R_s I$ is the applied voltage V minus the voltage that drops over the graphene (series) resistance R_s. The $R_s I$ term becomes relevant when the out-of-plane resistance of Au / P3HT / Gr is comparable to R_s, which typically happens for $V < -5V$ and device diameter larger than $10\,\mu m$ (see Fig. 47). At lower bias voltage, the J-V traces do not agree anymore with the TE model, but they show the typical trap free Space-Charge-Limited (SCL)[150,158,159] dependency where, on the one hand, if the charge carrier density at the contact N_0 is larger than $\sqrt{J\epsilon_0\epsilon_r/2\mu t q^2}$, where is the charge carrier mobility of the organic semiconductor, then

$$J = \frac{9}{8}\epsilon_0\epsilon_r\mu\frac{V^2}{t^3} \qquad (7)$$

and on the other hand, if N_0 smaller than $\sqrt{J\epsilon_0\epsilon_r/2\mu t q^2}$ then

$$J = q\mu N_0 \frac{V}{t} \qquad (8)$$

From Eq. 6, 7 and 8, one can extract the barrier height, the mobility, and the charge carrier density at the interfaces, provided knowledge of ϵ_r and A^{**}. The effective Richardson constant A^{**} can be obtained from temperature-dependent measurements through the Richardson plot ($\ln(J/T^2)$ vs. $1/T$), while the dielectric permittivity ϵ_r can be either taken from literature or extracted from capacitive measurements under hypothesis of fully depleted semiconductor. Since the extraction of the barriers height is sensitive to ϵ_r and since the latter depends on the measurement environment, it is beneficial to measure the dielectric permittivity of P3HT

on the system under study, if possible. Given that the charge carrier density of un-intentionally doped organic P3HT films is typically in the range of $1 \times 10^{17}\,\mathrm{cm}^{-3}$ to $1 \times 10^{18}\,\mathrm{cm}^{-3}$,[147,149] and that the doping concentration is usually reduced to roughly $1 \times 10^{15}\,\mathrm{cm}^{-3}$ by annealing in vacuum,[149,160] the P3HT can be safely assumed fully depleted and therefore ϵ_r extracted from impedance spectroscopy. This hypothesis can be assessed by measuring the capacitance of the heterostructure as a function of the applied bias: if the capacitance does not depend on the bias, then the depletion region extends over the entire thickness of the device.

A was extracted from the Richardson plot of a representative device having diameter of $5\,\mu\mathrm{m}$ at bias ± 5 V, such that the graphene series resistance Rs was negligible compared to the out-of-plane resistance of the stack and therefore $V' \pm 5\ V = V \pm 5$ V. Figure 20d shows the J-V characteristics as a function of temperature, from $200\,\mathrm{K}$ to $300\,\mathrm{K}$ in steps of $5\,\mathrm{K}$. The current density increases with temperature, peaking at -10 V from $1 \times 10^4\,\mathrm{A/m^2}$ (200 K) to $9.5 \times 10^4\,\mathrm{Am}^{-2}$, (300 K) while the J-Vs exhibit the typical exponential character of the TE model over the whole temperature range. The inset of Figure 20d shows the Richardson plot for bias 5 V (hole injection from Gr) and bias -5 V (hole injection from Au). From the intercept of the linear fit, the reduced effective Richardson constants results in $A^{**}_{Gr/P3HT} = 4.3\,\mathrm{Am}^{-2}\mathrm{K}^{-2}$ for hole injection from Gr and $A^{**}_{Au/P3HT} = 20.5\,\mathrm{Am}^{-2}\mathrm{K}^{-2}$ for hole injection from Au, similar to the values previously reported for metal / OSC[155,156] and Gr / OSC[50] interfaces. It is worth observing that A^{**} could be extracted from the Richardson plot in the whole voltage range where the J-V is exponential and R_s is negligible. However, Figure 48 shows that: (i) A^{**} does not vary significantly in that voltage range, and (ii) that the potential barriers height extracted from the fittings do not depend significantly on the particular choice of A^{**}. Therefore, the chosen values of A^{**} did not affect the results of this work.
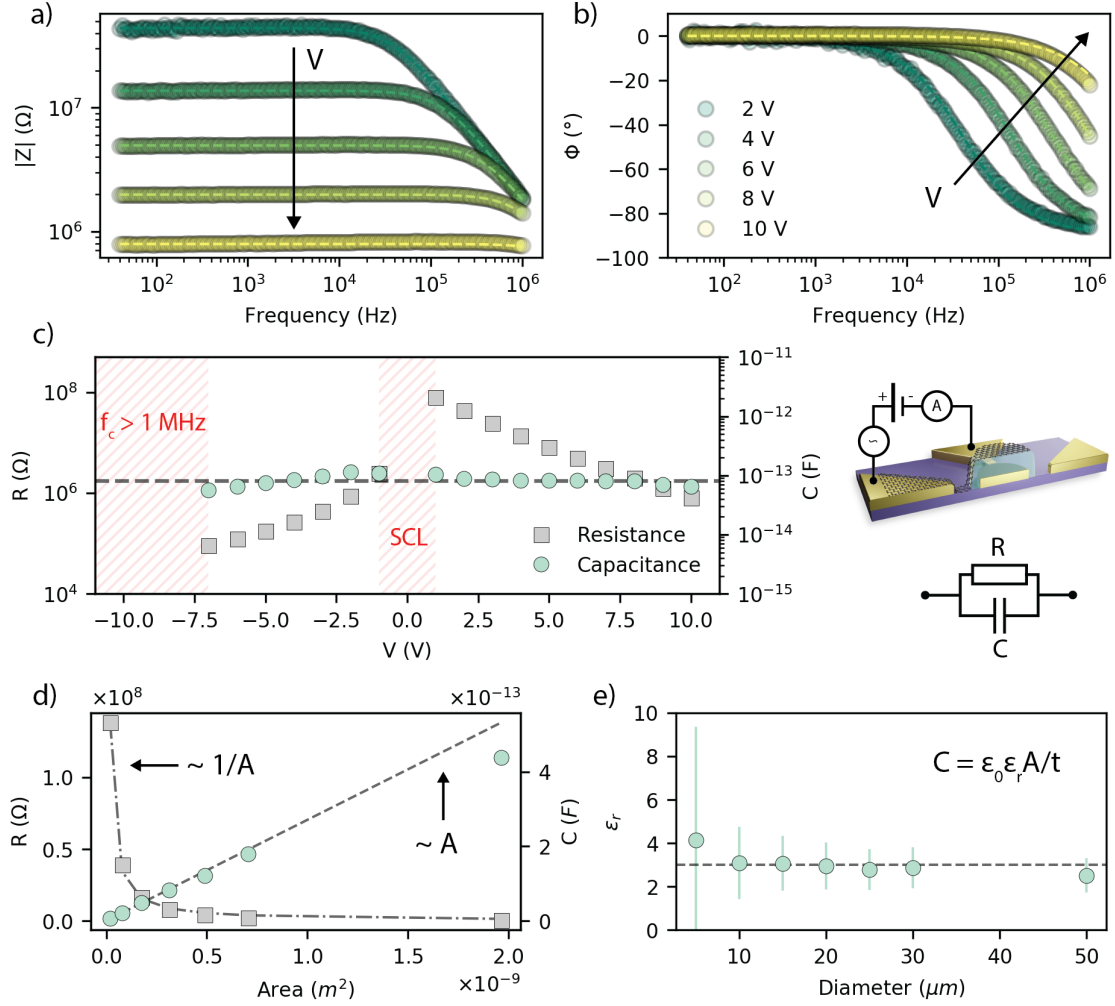
Figure 21: Impedance analysis. Modulus (a) and phase (b) of a representative 20 μm device: data (circles), $R||C$ model fit (dashed lines) (c) Resistance R and capacitance C extracted from the $R||C$ model fit at different biases. R and C are not calculated in the SCL region and for $V < -7.5$ V, where the cut-off frequency f_c is outside the measurement range. (d) Extracted R and C values for the devices with diameter: 5, 10, 15, 20, 25, 30 and 50 μm. The green dashed line is the linear fit of the capacitance vs. area. (e) ϵ_r vs. device diameter (error bars calculated as described in the supporting information).

The dielectric permittivity ϵ_r was extracted from the impedance spectroscopy on a representative device per device area. Figures 21a-b show the impedance of a representative device having diameter of 20 μm, in the frequency range 40 Hz – 1 MHz, for positive bias (refer to the supporting information for the impedance for negative biases). The impedance exhibits the typical behavior of an $R||C$ circuit. The resistance R and the capacitance C of the system are therefore extracted by fitting the experimental data with a non-ideal capacitor model $R||C$, and are re-

ported in Figure 21c. The high negative voltage range corresponding to $V < -7\,\mathrm{V}$ was not fitted because the cut-off frequency of the system is beyond $1\,\mathrm{MHz}$ (upper limit of the measurement range). The low voltage region ($|V| < 1\,\mathrm{V}$) was also not considered because the space-charge would result in a capacitance $3/2$ larger than the geometrical one.[159] The resistance decreases with the applied bias, from $80.7\,\mathrm{M\Omega}$ at $1\,\mathrm{V}$ to $791\,\mathrm{k\Omega}$ at $10\,\mathrm{V}$, possibly due to the image-charge-induced potential barrier lowering, while the capacitance is bias-independent around $80\,\mathrm{fF}$, confirming that the organic semiconductor is fully depleted.[161] The dielectric constant of P3HT is estimated from the geometrical capacitance (i.e. $C = \epsilon_0 \epsilon_r A / t$, where A is the area of the graphene electrode), without considering the edge effects and assuming a nominal thickness of $100\,\mathrm{nm}$ (see Fig. 42), resulting in $\epsilon_r \approx 3$, in agreement with previously reported values for P3HT.[19, 152–154] Figure 21d shows that the resistance and the capacitance scale as $1/A$ and A, respectively. It is worth observing that the dielectric constant calculated for small devices is affected from large error due to geometrical variability as reported in Fig. 21e.
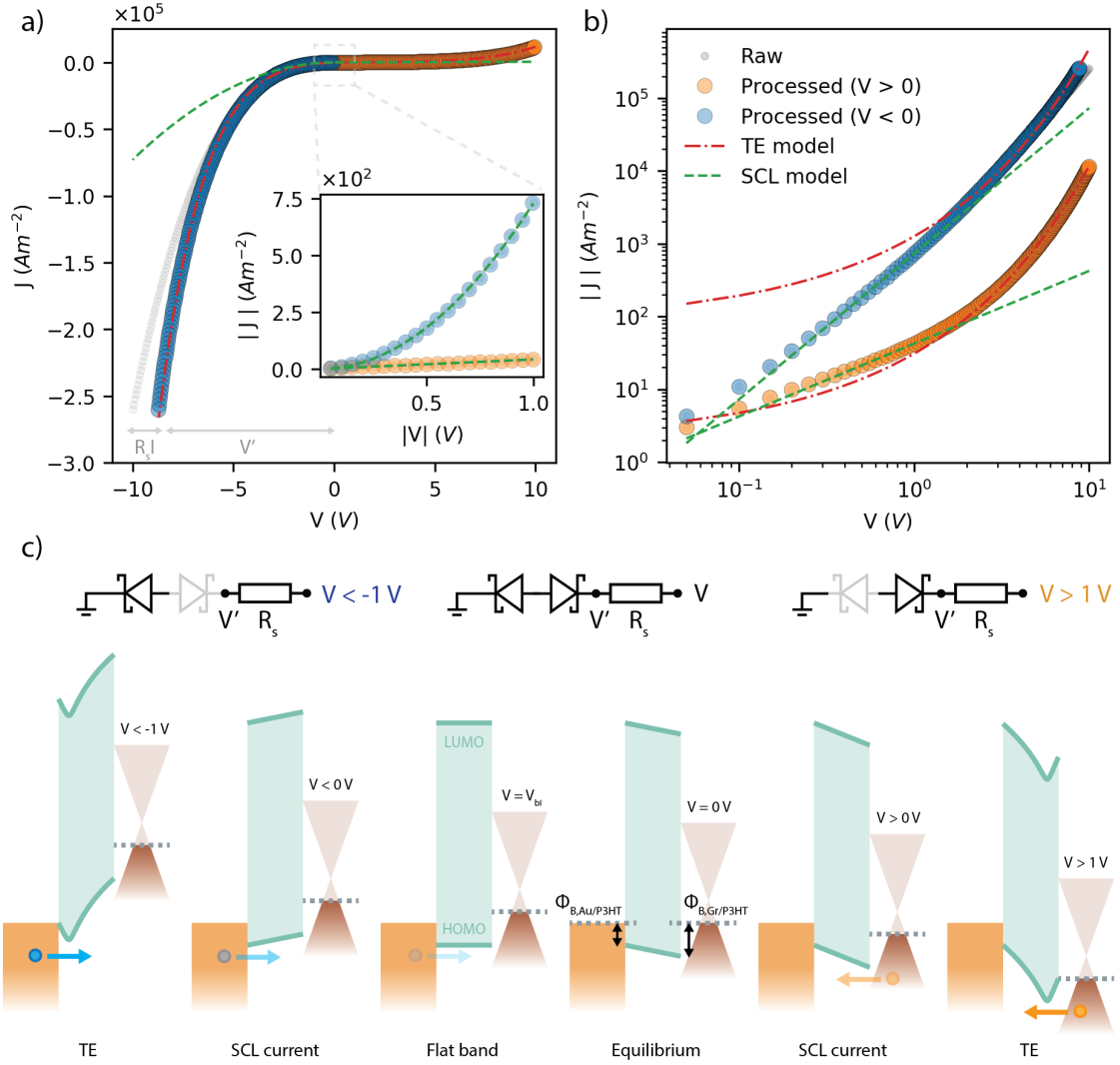
Figure 22: (a) Current density across a 20 µm large Au / P3HT / Gr device. Experimental data are represented by small grey circles. Corrected data (orange and blue large circles) takes into account for the graphene series resistance. The graph shows the fitting results of the SCL current (green dashed lines) and TE (blue dashed lines). The inset shows the $\pm 1\,\text{V}$ region where the space-charge effect is limiting the current across the heterostructure. (b) Current density shown in (a) but in logarithmic scale. Current density for positive and negative biases is represented by orange and blue circles, respectively. (c) Band diagram of the Au / P3HT / Gr heterojunction illustrating the charge transport regimes.

Given A^{**} and ϵ_r, one can finally use Eq. 6, 7 and 8 to fit the experimental J-Vs and extract ϕ_B, μ, and N_0, as anticipated above. Figure 22a shows the J-V curve of a representative device having diameter of 20 µm. The grey circles represent the raw data, while the orange and blue circles are the processed data for the positive and negative biases, respectively, where V is replaced by $V' = V - R_s I$. The

barrier height and R_s are obtained by a parametric fit of the TE model (Eq. 6) in R_s of the processed data in the high voltage regime ($|V| > 1\,\text{V}$), where R_s spans the interval 0-100 kΩ in steps of 100 Ω. The fit result in $R_s = 15.4\,\text{k}\Omega$, $\phi_{B,Gr/P3HT} = 0.31\,\text{eV}$ and $\phi_{B,Au/P3HT} = 0.25\,\text{eV}$, giving a built-in potential of about 60 meV. The barriers height measured by KPFM in ambient on a representative device resulted in $\phi_{B,Au/P3HT}^{KPFM} = 0.10 \pm 0.03$ eV and $\phi_{B,Gr/P3HT}^{KPFM} = 0.16 \pm 0.03$ eV, which differ from those extracted from the fit of the J-Vs, although follow the same trend $\phi_{B,Gr/P3HT}^{KPFM} > \phi_{B,Au/P3HT}^{KPFM}$ (refer to the Appendix D for details on the KPFM measurements). This inconsistency should not surprise, as the KPFM strongly depends on the purity of the surface and therefore on the measuring environment,[162] which differ from the environment of the J-V measurements. Nevertheless, the built-in potential measured by KPFM matches the value obtained from the fitting of the J-V curves. This could be ascribed to a similar shift in the graphene and gold work functions, such that the built-in potential of the stack depends mostly on the doping ofP3HT when exposed to air.[147,148] It is worth observing that $\phi_{B,Au/P3HT}^{KPFM}$ differs from previously reported values for Au / P3HT interfaces measured with other techniques or in different environments,[163,164] ultimately pointing to the fact that the estimation of the barrier height is very sensitive to both the measurement conditions and the measurement method. The inset of Figure 22a shows the current density in the low voltage regime ($|V| < 1\,\text{V}$). Since the built-in potential is very small, the flat-band condition is very close to the equilibrium condition. Therefore, the SCL is observed for small biases, in agreement with Eq. 7. Fitting the current density for negative biases with Eq. 7 results in an out-of-plane hole mobility of $\mu \approx 2.4 \times 10^{-4}\,\text{cm}^2\text{V}^{-1}\text{s}^{-1}$, similar to previously reported values for in-plane hole mobility in P3HT.[149,160] Fitting the current density for positive biases with Eq. 8 gives the density of charge carriers at the Gr / P3HT interface, which corresponds to the intrinsic carrier concentration of P3HT (see Appendix D). This results in $N_0 \approx 1.1 \times 10^{15}\,\text{cm}^{-3}$, also in agreement with previously reported value for intrinsic P3HT in vacuum.[149,160] In the SCL model, the charge carrier density at the contacts depends on the density of states in the semiconductor and on the potential barrier height at the interface. From N_0, one can therefore calculate the charge carrier density at the Au / P3HT interface, resulting in $\approx 1.2 \times 10^{16}\,\text{cm}^{-3}$. The difference between $N_{0,Au/P3HT}$ and $N_{0,Gr/P3HT}$, is in agreement with the experimental evidence that $J \approx V$ for positive bias and $J \approx V^2$ for negative bias (see the Appendix D for a discussion). The J-Vs dependency are especially clear in the inset of Figure 22a and in Figure 22b.

Figure 22c shows the energy band diagram of the Au / P3HT / Gr heterostructure

sketched using the barrier heights extracted from the fit of the J-Vs, and assuming that the P3HT is fully depleted, as proven by capacitive measurements. The curvature of the HOMO and LUMO levels in proximity of the interfaces qualitatively describes the potential barrier lowering due to image charge effect. The Fermi level of P3HT lies close to the HOMO level, as expected from Fermi level pinning due to interface states.[106, 165]

d	t	Space-charge model ($|V| < 1V$)		Thermionic emission model ($|V| > 1V$)		
		N_0	μ	R_s	$\Phi_{B,Gr/P3HT}$	$\Phi_{B,Au/P3HT}$
(μm)	(nm)	($1 \times 10^{15}\,\mathrm{cm}^{-3}$)	($1 \times 10^{-4}\,\mathrm{cm}^{-2}\mathrm{V}^{-1}\mathrm{s}^{-1}$)	kΩ	(eV)	(eV)
5	130	0.94 ± 0.40	4.36 ± 0.61	35 (fixed)	0.30 ± 0.02	0.25 ± 0.01
10	120	1.14 ± 0.12	3.72 ± 0.92	35 (fixed)	0.29 ± 0.01	0.25 ± 0.01
15	100	1.11 ± 0.26	2.26 ± 0.21	42.0 ± 7.9	0.31 ± 0.01	0.26 ± 0.01
20	100	1.13 ± 0.26	2.37 ± 0.09	19.1 ± 10.9	0.31 ± 0.01	0.25 ± 0.01
25	100	1.44 ± 0.37	2.41 ± 0.21	24.6 ± 16.5	0.30 ± 0.01	0.25 ± 0.01
35	100	1.16 ± 0.26	2.13 ± 0.08	12.7 ± 6.4	0.30 ± 0.01	0.25 ± 0.01
50	100	1.20 ± 0.14	2.32 ± 0.09	11.2 ± 12.8	0.29 ± 0.01	0.25 ± 0.01
all	100	1.16 ± 0.65	2.80 ± 2.17	25.6 ± 24.3	0.30 ± 0.02	0.25 ± 0.02

Table 2: Statistics of the Fitting Parameters. The average on five devices is given for N_0, μ, R_s, and Φ. The reported error is the min/max value.All SCL and TE model fits were done using $\epsilon_r \approx 3$, $A^{**}_{Gr/P3HT} = 4.3\,\mathrm{Am}^{-2}\mathrm{K}^{-2}$ and $A^{**}_{Au/P3HT} = 20.5\,\mathrm{Am}^{-2}\mathrm{K}^{-2}$. The series resistance of the 5 μm and 10 μm devices is very small compared to the device out-of-plane resistance. In order to prevent the fitting algorithm to maximize R_s, the latter was set to 35 kΩ for 5 μm and 10 μm devices. Figure S5 shows the current density and the fits of various devices.

6.4 Conclusion

This work demonstrates a potentially upscalable fabrication process for Au / P3HT / Gr VdW heterostructures on Si / SiO$_2$ and describes the charge injection and transport mechanism across the heterostructures. The device output characteristic is independent from the device size for device diameters from 50 μm down to 5 μm, making device downscaling accessible and possibly limited solely by lithography resolution.

Impedance spectroscopy measurements shows that the P3HT is fully depleted in the high bias regime ($|V| > 1$ V or $|V|/t > 10$ MV m^{-1}) and therefore the dielectric constant of P3HT is determined from the geometrical capacitance of the devices, resulting in $\epsilon_r \approx 3$. The electrical transport measurements show that the charge injection across the Au / P3HT and Gr / P3HT interfaces is dominated by TE in the high bias regime ($|V| > 1$ V), with potential barriers of $\Phi_{B,Gr/P3HT} = 0.30$ eV and $\Phi_{B,Au/P3HT} = 0.25$ eV, respectively, and by SCL current in the low bias regimes ($|V| < 1$ V). The intrinsic carrier concentration and the out-of-plane hole mobility of P3HT, determined by fitting the J-Vs in the low bias regime with the SCL model, resulted in $\mu \approx 2.8 \times 10^{-4}$ cm^{2}V^{-1}s^{-1} and $N_0 \approx 1.16 \times 10^{15}$ cm^{-3}, similar to literature values extracted from in-plane FET measurements. The energy band diagram of the heterostructure shows that the interface traps/defects pin the Fermi level very close to the HOMO level of P3HT. Since the current in Au / P3HT / Gr heterostructures is injection-limited, the hole mobility of P3HT does not limit the operating frequency of the stack, which exceeds 1 MHz for bias approaching 10 V. Higher cutoff frequencies could be achieved by making Ohmic the contact between the electrodes and P3HT, for instance by introducing a (heavily) doped OSC layer between the electrodes and the OSC, such as F4TCNQ- or F6TCNNQ-doped P3HT.

Overall, this work shows that graphene can be implemented as top or inter-layer electrode in vertical devices based on multi-layer Van der Waals heterostructures. For instance, the charge injection between gold and P3HT could be optimized to achieve high operating frequencies, while the Gr / P3HT interface kept as is to exploit its rectifying nature. With graphene acting as a permeable electrode, the Gr / P3HT heterostructure studied in this work could become the core element to build future vertical organic transistors based on two back-to-back Gr / P3HT diodes.

7 Field- and Thermal-Emission Limited Charge Injection in Au-C60-Graphene van der Waals Vertical Heterostructures

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Author contributions

Abstract

Among the family of 2D materials, graphene is the ideal candidate as top or interlayer electrode for hybrid van der Waals heterostructures made of organic thin films and 2D materials due to its high conductivity and mobility, and its inherent ability of forming neat interfaces without diffusing in the adjacent organic layer. Understanding the charge injection mechanism at graphene/organic semiconductor interfaces is therefore crucial to develop new organic electronic devices. In particular, Gr / C60 interfaces are promising building blocks for future n-type vertical organic transistors exploiting graphene as tunneling base electrode in a two back-to-back Gr / C60 Schottky diodes configuration. This work delves into the charge transport mechanism across Au / C60 / Gr vertical heterostructures fabricated on Si/SiO$_2$ using a combination of techniques commonly used in the semiconductor industry, where a resist-free CVD graphene layer functions as top electrode. Temperature-dependent electrical measurements show that the transport mechanism is injection limited and occurs via Fowler-Nordheim tunneling at low-temperature, while it is dominated by a non-ideal thermionic emission at room and high temperatures, with energy barriers at room temperature of ca. $0.58\,\mathrm{eV}$ and $0.65\,\mathrm{eV}$ at the Gr / C60 and Au/C60 interfaces, respectively. Impedance spectroscopy confirms that the organic semiconductor is depleted and the energy band diagram results in two electron blocking interfaces. The resulting rectifying nature of the Gr / C60 interface could be exploited in organic hot electron transistors and vertical organic permeable-base transistors.

7.1 Introduction

Graphene is the ideal candidate as top or interlayer electrode for hybrid van der Waals heterostructures made of organic thin films and 2D materials due to its high conductivity and mobility, and its inherent ability of forming neat interfaces without diffusing in the adjacent organic layer, in contrast to commonly used metal electrodes.[81] Graphene-organic hybrid devices have been widely explored[1] for their potential use in various applications, including organic light-emitting diodes,[137,138] organic photovoltaics,[133,134] and vertical organic transistors.[24,51,52,55,95,97] Nevertheless, new techniques and large-area fabrication methods still needs to be developed for effectively incorporating graphene as a top and/or interlayer electrode in hybrid organic devices. In fact, graphene is typically implemented as a gateable bottom electrode into barristors.[24,51,52,55,95,97] However, more complex multilayer architectures could exploit the unique properties of graphene, i.e. optical transparency,[166] flexibility,[167] and ability to conform to three-dimensional and/or rough surfaces.[168] For instance, graphene could be implemented as the base electrode in organic hot electron transistors, where ultra-thin organic layers are required, or replace the metallic base electrode in vertical organic permeable-base transistors.[61,70] This would enable flexible vertical organic transistors operating at high frequencies[75] that are suitable for applications such as wearable electronics with communication functions, or RF tags. Flexible vertical transistors could also be vertically integrated in OLEDs,[70] enabling high resolution organic displays with enhanced contrast. Within this framework, understanding the charge transport mechanisms occurring at the interface between graphene and Organic Semiconductor (OSC) is crucial for the development of new graphene-based optoelectronic devices.[1,5,140]

The fabrication techniques presented in this work are similar to what previously reported for vertical vdW heterostructures made of the p-type polymer P3HT and CVD grown graphene.[82] In this case, however, the graphene sheet is transferred on top of a thermally evaporated thin film of small molecules, i.e. the n-type organic semiconductor C60, and subsequently patterned into the top electrode. The fabrication processes combines techniques commonly used in the semiconductor industry, and therefore it can be up-scaled to wafer-level. The charge injection mechanisms at the interfaces, i.e. Gr / C60 and Au / C60, are investigated by temperature-dependent I-V measurements and impedance spectroscopy. The current-voltage characteristic is modeled by the Double Schottky Barrier (DSB) model at room and high temperature (above $300\,\mathrm{K}$) and by FN tunneling at low temperature (below $100\,\mathrm{K}$). The energy barriers height at the Gr / C60 and Au / C60 interfaces is extracted from the DSB and from the FN tunneling models, while the static dielectric

constant of C60 is determined by impedance spectroscopy. The study concludes with the energy band diagram of the heterostructure explaining the charge injection at the two interfaces.

7.2   Results and Discussion
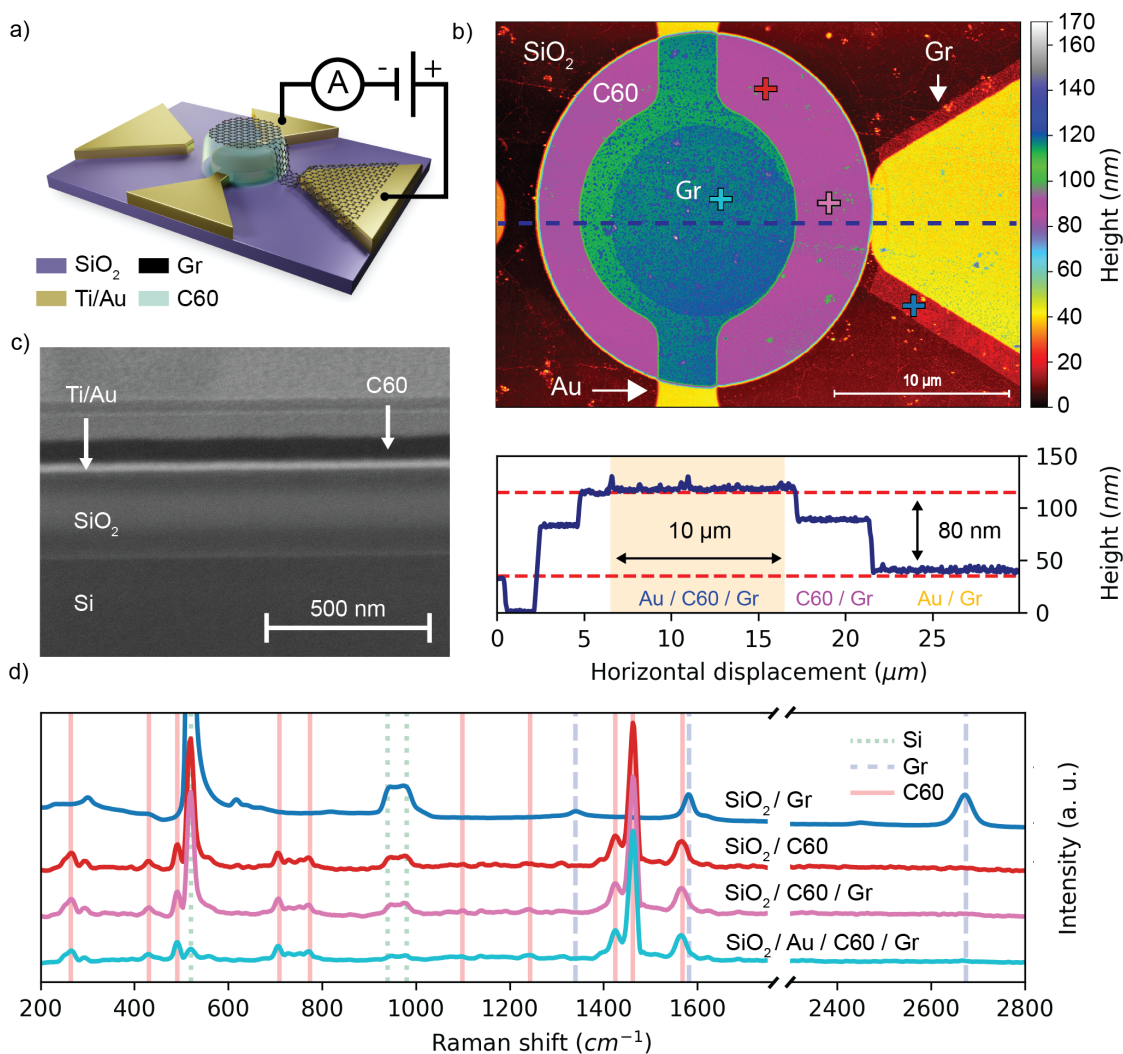
Figure 23: (a) 3D schematic of the Au / C60 / Gr vertical heterostructure (not to scale). Adapted from Oswald, J. et al. ACS Appl. Mater. Interfaces 2022.[82] (b) AFM height image and profile of a representative 10 µm device. (c) Cross-section SEM image of the Au / C60 / Gr heterostructure cut at the center of the graphene top electrode, parallel to the AFM profile shown in (b). (d) Raman spectra taken at different locations of the device, marked by colored crosses in Figure 23b. The vertical lines with different colors refer to the characteristic Raman peaks of Si, Gr and C60.

This study was performed on one chip that includes two distinct groups of devices: (i) 119 Au / C60 / Gr Vertical Stacks, with diameters spanning from 5 µm to 50 µm and C60 film thickness of 80 nm, and (ii) 34 Graphene Bridges to characterize the in-plane resistance of graphene after transfer on C60. Figure 23a shows the 3D schematic of the Au / C60 / Gr Vertical Stack, fabricated following the protocol reported in the Experimental Methods and in Appendix E, together with the electrical scheme implemented for the measurements, while the schematic of the Graphene Bridge and the corresponding electrical scheme is shown in Appendix E (Fig. 52). Figure 23b shows the AFM height image and height profile of a representative Vertical Stack having a diameter of 10 µm. From the AFM height image one can extract the actual diameter of the graphene electrode (i.e. 10 µm), while the height profile shows the thickness of the bottom electrodes (35 nm) and of C60 (80 nm). Refer to Appendix Appendix E for the AFM height image of a representative Graphene Bridge device (Fig. 52). Figure 23c shows a cross-section of the Au / C60 / Gr stack, where the four visible layers are Si (525 µm), SiO_2 (335 nm), Ti/Au (5 nm / 30 nm), and C60 (80 nm). The resolution of the instrument does not allow to observe the graphene electrode on top of the stack. Figure 23d shows the Raman spectra taken at different locations of the device, marked by colored crosses in Figure 23b. The Raman spectrum of CVD graphene (SiO_2/Gr) shows the characteristic G (1582 cm^{-1}) and 2D (2674 cm^{-1}) peaks, as well as the D (1340 cm^{-1}) peak, with a weak amplitude, possibly resulting from fabrication-induced defects. The C60 film (SiO_2/C60), the C60 film covered by graphene (SiO_2/C60/Gr) and the full stack (SiO_2/Au/C60/Gr) Raman spectra are virtually identical and display the characteristic Raman active vibrations of C60,[114] i.e., Hg(1) at 264 cm^{-1}, Hg(2) at 431 cm^{-1}, Ag(1) at 492 cm^{-1}, Hg(3) at 709 cm^{-1}, Hg(4) at 774 cm^{-1}, Hg(5) at 1099 cm^{-1}, Hg(6) at 1244 cm^{-1}, Ag(2) at 1463 cm^{-1} and Hg(8) at 1568 cm^{-1}. The typical Raman scattering of Si,[113] i.e. the first-order optical mode (520 cm^{-1}) and second-order scattering band (940 cm^{-1} – 980 cm^{-1} cm-1), due to the Si substrate, are observed in all spectra. The results of the AFM, SEM and Raman analysis show that the methods used to fabricate the vertical vdW devices are compatible with Graphene and C60 and do not degrade these materials.
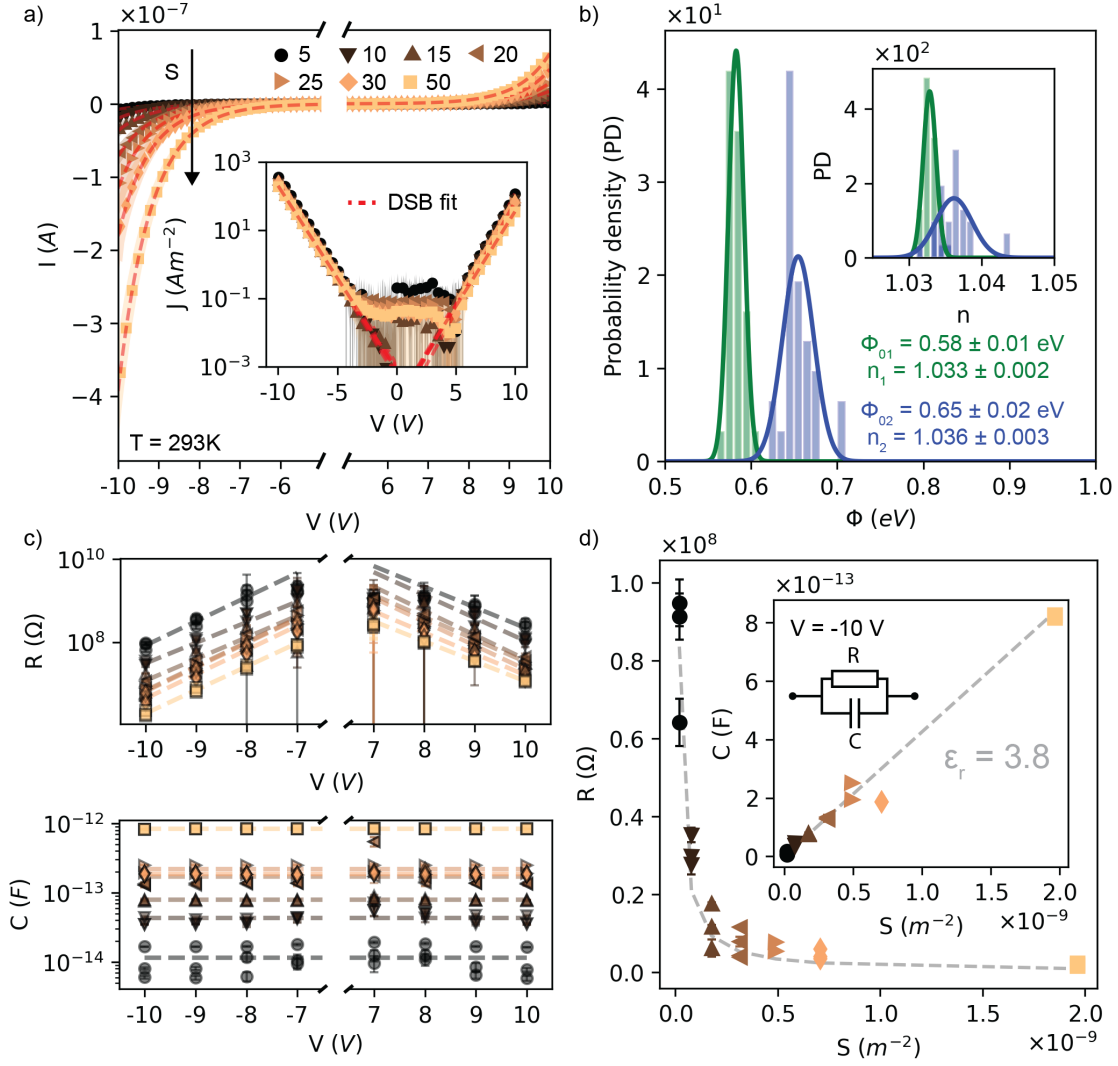
Figure 24: Electrical measurements under vacuum ($\approx 1 \times 10^{-6}$ mbar) at room temperature ($293\,\mathrm{K}$). (a) Average of the current-voltage characteristics measured on 5 devices for each diameter: 5, 10, 15, 20, 25, 30, and $50\,\mu\mathrm{m}$. The shaded area represents the standard deviation. The dashed red line is the average of the DSB fits on 5 devices per area. The figure does not display the I-V data in the range from $-5\,\mathrm{V}$ to $5\,\mathrm{V}$, where the current is below the sensitivity of the instrument. The inset shows the J-Vs on the whole measurement range. (b) Distribution of $\Phi_{01,02}$ and $n_{1,2}$ extracted from the DSB on 35 device (5 devices for each diameter), associated to the Gr / C60 and Au / C60 interfaces, respectively. (c) Resistance R and capacitance C vs. applied bias, extracted from the fit of the non-ideal capacitor model. The dashed lines are the linear fit of R and C versus bias. (d) Scaling of R and C with device area. The inset shows the capacitance C vs. the device area S. The grey dashed lines represent the capacitance $C = \epsilon_0 \epsilon_r S / t$, where $\epsilon_r = 3.8$ is the deduced static dielectric constant of C60, and the resistance R which scales as $1/S$.

The effects of the environment and of the device area on the charge transport are investigated by comparing the I-V characteristics measured in air and vacuum, and by studying the scaling relationship between the system resistance and capacitance and the device area, where the device resistance and capacitance are obtained from impedance measurements under vacuum. In addition, by examining the correlation between the applied voltage and the system capacitance, it is possible to determine whether the OSC is fully depleted and to exclude the possibility of electrostatic doping in graphene. Oxygen and moisture are known to affect the electrical properties of C60 and graphene.[107–109,169–171] In particular, oxygen and moisture typically act as electron trap centers for C60, reducing the electrical conductivity of the film,[169–171] while they typically *p*-dope graphene on SiO_2,[107–109] as shown in Appendix E for the Graphene Bridges devices (Fig. 53, Table 5) and as demonstrated on graphene field effect transistors (Fig. 54). In order to desorb oxygen and water from C60 and from the graphene surface, and therefore ensure the consistency and reproducibility of measurements done in different systems, all measurements are done in vacuum after annealing (Fig. 55). Figure 24a shows the average I-V traces of 5 devices per area measured under vacuum ($\approx 1 \times 10^{-6}$ mbar) at room temperature (293 K) after annealing for 12 h at 110 °C. To the purpose of clarity, the figure does not display the I-V data in the range from -5 V to 5 V, where the current is below the sensitivity of the instrument. The inset of Figure 24a shows that the J-V traces of all devices overlap, and thus, that the transport characteristic is not affected by the device area. The small variability between J-Vs is ascribed to the device inhomogeneities due to the fabrication. After annealing, the J-V characteristics become very similar, while a larger variability is observed for the J-V traces taken in air and shown in Appendix E (Fig. 56). Interestingly, the stacks become less conductive in vacuum after annealing (Fig. 55), against what one would expect if the charge transport were bulk limited by C60 due to oxygen and moisture desorption. This observation suggests that the transport is not bulk-limited but injection-limited, and that the oxygen and moisture have an impact on the energetics of the interfaces. All J-Vs display the same non-linear and asymmetric s-shaped characteristic: the current initially increases slowly with increasing voltage and then rapidly increases at higher voltages; the same occurs for negative voltages, but the magnitude of the current is higher. Similar trends are typically described by various analytical models for the charge injection at the metal/semiconductor interface, i.e. termionic emission (TE),[150] the Modified TE (MTE) developed for graphene/semiconductor interfaces,[50,151] direct tunneling and Fowler-Nordheim (FN) tunneling.[150] However, in most cases the charge injection at the metal/OSC follows a hybrid process,[156]

which includes tunneling and thermionic emission[48] with deviations from the standard theory due to defects, surface inhomogeneity and image-charge barrier lowering, resulting in a bias dependent barrier height.[150,172] This hybrid process can be described by a non-ideal Schottky diode model with ideality factor n,[150] where the reverse current is $I = SA^{**}T^2 \exp\left(-\Phi/kT\right)$, and where S is the contact area, T is the absolute temperature, A^{**} is the reduced effective Richardson constant, k is the Boltzmann constant, and $\Phi = \Phi_0 \pm (1 - 1/n)qV$ is the voltage-dependent energy barrier with nominal barrier height Φ_0 and ideality factor n, and where q is the elementary charge. The model can be extended to a double barrier system, where different potential barrier heights are formed at two interfaces in series. This model is called Double Schottky Barrier (DSB) model and is described by[172]

$$I_T = \frac{2I_{S1}I_{S2}\sinh\left(-\frac{qV}{2kT}\right)}{I_{S1}\exp\left(\frac{qV}{2kT}\right) + I_{S2}\exp\left(-\frac{qV}{2kT}\right)} \tag{9}$$

With reference to the Au / C60 / Gr Vertical Stacks of this work, $I_{S1,2} = S_{1,2}A^{**}T^2\exp\left(-\Phi_{1,2}/kT\right)$ are the reverse saturation currents, and $\Phi_{1,2} = \Phi_{01,02} \pm (1 - 1/n_{1,2})qV$ are the voltage dependent energy barriers at the Gr / C60 and Au / C60 interfaces, respectively. In this model, the current is limited by the reverse currents. When $V > 0$, the Gr / C60 diode (SB_1) is forward biased and the Au / C60 diode (SB_2) is reversed biased. Therefore, the measured current is mostly given by the reverse current of SB_2, i.e. I_{S2}. On the contrary, when $V < 0$, the current is limited by SB_1, i.e. I_{S1}. The DSB model is applied to the I-Vs in Figure 24a considering two different contact surfaces, i.e. $S_1 = \pi(d_1/2)^2$ for the graphene top electrode and $S_2 = \pi(d_2/2)^2$ for the Au bottom electrode, where d_1 and d_2 are the diameter of the contact area and d_2 is $2\,\mu m$ larger than d_1, while the reduced effective Richardson constant for both interface is set to $A^{**} = 100\,\mathrm{Am^{-2}K^{-1}}$. It is worth observing that A^{**} is extracted from temperature-dependent measurements and it varies in the range $1 \times 10^{-1}\,\mathrm{Am^{-2}K^{-1}}$ - $1 \times 10^3\,\mathrm{Am^{-2}K^{-1}}$ depending on the device and voltage (refer to Appendix E, Fig. 57-58 and Table 6), as typically reported for metal / OSC interfaces.[155,156] The variation of the energy barriers extracted with different A^{**} from the aforementioned range is less than $0.1\,eV$ (as shown in Appendix E, Fig. 59), and it does not affect the conclusions of this work. Figure 24a shows the DSB fits (red dashed line) of the experimental data. The dashed red line is the average of the DSB fits on 5 devices per area (the fits of the individual traces are shown in Appendix E, Fig. 60). Figure 24b shows the distributions of the energy barriers $\Phi_{01,02}$ and ideality factors $n_{1,2}$ of the Gr / C60 and Au / C60 interfaces, respectively. The normal distributions are given by $\Phi_{01} = (0.58 \pm 0.01)\,eV$,

$\Phi_{02} = (0.65 \pm 0.02)\,\text{eV}$, $n_1 = 1.033 \pm 0.002$ and $n_2 = 1.036 \pm 0.003$. The potential barrier height of the Au / C60 interface is similar to previously reported value for C60 field-effect transistors with Au electrodes.[173] Impedance spectroscopy reveals that the Vertical Stacks exhibit the typical non-ideal capacitor characteristics. Figure 24c shows the average (on three devices per device area) resistance R and capacitance C of the Vertical Stacks obtained from impedance spectroscopy by fitting the modulus and phase with a non-ideal capacitor model, i.e. an $R//C$ circuit. Refer to Appendix E for details on the fit (Fig. 61). The resistance depends on the applied bias, as expected from the I-V characteristics, while the capacitance is bias-independent, therefore suggesting that the C60 is fully depleted[161] and that the voltage drops linearly over the whole structure. As a consequence, the electrostatic doping of graphene (i.e. Fermi energy E_F shift of graphene induced by the applied bias) predicted by the MTE[50] can be discarded, and the position of the E_F of the graphene electrode is determined solely by the chemical doping of graphene. It is known that C60 adsorbed on graphene typically results in p-doping.[120] This is demonstrated by a comparison between field-effect measurements on a set of Gr channels before and after deposition of C60, in Appendix E (Fig. 54). The charge neutrality point of the graphene field transistors shifts to positive gate biases (ca. 20 V) when a thin film of C60 is deposited on top of graphene, resulting in an average p-doping of about $1.4 \times 10^{12}\,\text{cm}^{-2}$ (refer to Appendix E, Eq. 33). Figure 24d shows the device resistance and capacitance versus area at a fixed bias of $-10\,\text{V}$. The resistance scales as $1/S$, where S is the area of the top electrode, while the capacitance scales as S (grey dashed lines in Fig. 24d). The static dielectric constant of C60, $\epsilon_r = 3.8$, is determined from the geometrical capacitance of the device $C = \epsilon_0 \epsilon_r S / t$, where t is the thickness of the C60 film (80 nm) and ϵ_0 is the vacuum permittivity. This value is in agreement with previous works.[40,41] The results of the DSB analysis, supported by the impedance measurements, suggest that the vertical charge transport in the Au / C60 / Gr is limited by charge injection. Further insight on the energy barrier and charge injection mechanisms at the Gr / C60 and Au / C60 interfaces is obtained by temperature dependent measurements.
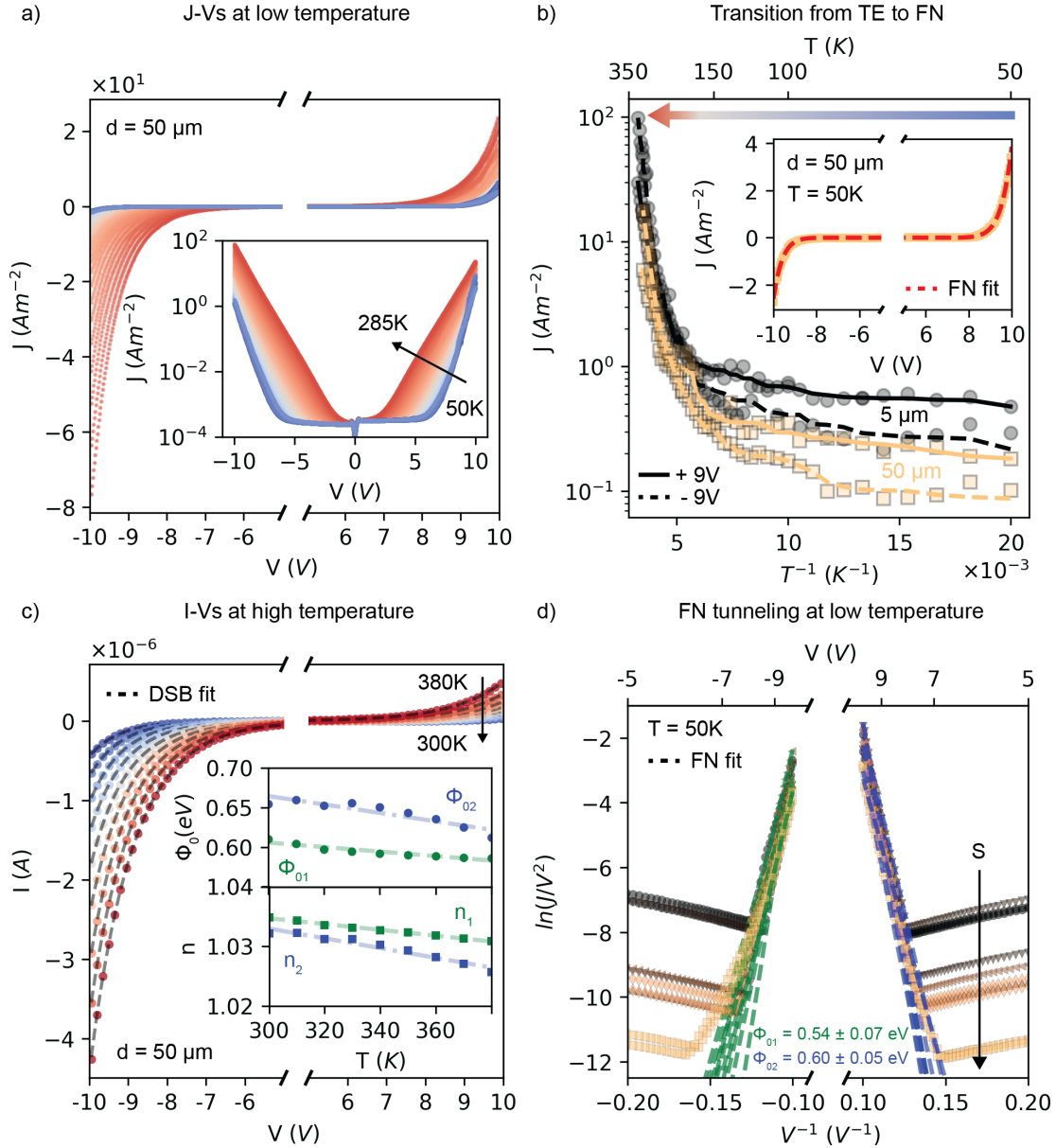
Figure 25: (a) Temperature dependent J-V characteristic of a representative $50\,\mu m$ device from $50\,K$ to $285\,K$. The inset shows the J-Vs on the whole measurement range. (b) Temperature dependent current density of two representative devices of $5\,\mu m$ and $50\,\mu m$ at fixed biases of $\pm 9\,V$. The inset shows the FN tunneling model fits for J-V data at $50\,K$. (c) Temperature dependent I-V characteristic of a representative $50\,\mu m$ device from $300\,K$ to $380\,K$ in steps of $10\,K$. The inset shows Φ_{01}, n_1 and Φ_{02}, n_2, extracted from the DSB model, as a function of temperature. (d) $\ln(J/V^2)$ vs. $1/V$ plot and FN fits (dashed lines) at $50\,K$ for a set of devices covering the whole diameter range, from $5\,\mu m$ to $50\,\mu m$. When $V < 0$, charge carriers tunnel through the energy barrier given by the Gr / C60 interface (SB_1), i.e. Φ_{01}. On the contrary, when $V > 0$, charge carriers tunnel through the energy barrier given by the Au / C60 (SB_2), i.e. Φ_{02}.

Temperature-dependent electrical measurements are necessary to distinguish the different charge injection mechanisms contributing to the electrical current in the devices and possibly explain the non-ideal thermionic emission observed at room temperature. Low and high temperature-dependent electrical measurements are done in two different systems as described in the Methods sections, and the results are shown in Figure 25. In particular: Figure 25a shows the J-V characteristics as a function of temperature of a representative 50 μm device, in linear and logarithmic scale, from 50 K to 285 K in steps of 5 K (similar data for a representative 5 μm device are shown in Appendix E, Fig. 62); Figure 25c shows the I-V characteristics for a representative 50 μm device as a function of temperature, from 300 K and 380 K in steps of 5 K; Figure 25b shows the current density at ±9 V for two representative devices belonging to the smallest (5 μm) and the largest set (50 μm), from 285 K to 50 K; and Figure 25d displays the analysis for the observed low temperature injection mechanism. Figure 25b shows that while the current density depends strongly on the temperature above 200 K, in agreement with a thermally activated charge injection mechanism, the temperature dependence becomes very weak below 200 K. The current becomes approximately temperature-independent below 100 K. Figure 25c shows the I-V characteristic of a representative 50 μm in the high temperature range between 300 K and 380 K. In this range, the charge injection is dominated by thermionic emission and the DSB model can fit all I-Vs. The inset of Figure 25c shows the energy barriers Φ_{01}, Φ_{02} and ideality factors n_1, n_2 as a function of temperature, extracted from the DSB fit for the Gr / C60 and Au / C60 interfaces, respectively. The ideality factor of both interfaces decreases with increasing temperature, indicating that the device approaches the ideal TE injection model at higher temperatures, with values around $n_1 = 1.026$ and $n_2 = 1.031$. Simultaneously, the potential barriers height decrease with temperature. This should not come as a surprise, as it is known that barrier inhomogeneity can lead to temperature-dependent energy barriers.[174,175] Below 100 K, the J-Vs are approximately temperature independent and well described by the FN tunneling mechanism under WKB (Wentzel-Kramers-Brillouin) approximation, in formula[150]

$$J = \frac{q^3(V/t)^2}{16\pi^2\hbar\Phi_{01,02}} \exp\left[\frac{-4t\sqrt{2m(\Phi_{01,02})^3}}{3\hbar qV}\right]$$

(10)

where m is the effective mass of the electron in the semiconductor and $\hbar$ is the reduced Plank constant. Here, the free electron mass is considered. The inset of Figure 25b shows representative J-V traces of a representative 50 μm device and the corresponding FN fit, while Figure 25d shows the $ln(J/V^2)$ vs. $1/V$ plot at

high bias (typically linear when $|V| > 8V$) for 5, 10, 15, 20, 25, 30 and 50 μm 10 representative devices at 50 K. The J-Vs are very similar, and the energy barrier of the two interfaces can be derived from the slope of the $ln(J/V^2)$ vs. $1/V$ plot at $|V| > 8V$, resulting in $\Phi_{01} = (0.54 \pm 0.07)\,eV$ and $\Phi_{02} = (0.60 \pm 0.05)\,eV$, which are similar to those obtained from the DSB model fit at high temperature. Refer to Appendix E (Fig. 63) for the I-V traces in the range from $-10\,V$ to $10\,V$. It is worth observing that the asymmetry of the J-Vs characteristics changes from high to low temperatures. In details, the rectification ratio at $\pm 9V$, that is $RR = |J(+9V)/J(-9V)|$, is ca. 1.14 at 50 K and 0.13 at 380 K. Although it is hard to explain quantitatively the phenomenon, one should observe that the injection mechanism changes from non-ideal TE at high temperature to FN tunneling at low temperatures, which are described by different models with different pre-factors. The latter are known to deviate significantly from theoretical values in non-ideal and/or metal/OSC systems.[155,156] A transition from FN to direct tunneling would only be possible with a thinner semiconductor. The C60 thickness for transition between FN tunneling and direct tunneling at room temperatures can be approximated by $t = \Phi_B/E$, where E is the electric field.[150] Assuming an energy barrier of 0.5 eV, which corresponds roughly to the measured value for the Gr/C60 interface, and an electric field of $E = 10\,V/80\,nm = 1.25\,MVcm^{-1}$, this results in a C60 thickness of $\approx 4\,nm$. Few-nm thin vertical stacks can be theoretically achieved using the architecture and fabrication process described in this work, where graphene is used as top electrode. In fact, this fabrication process allows to avoid the typical metal atoms intercalation and diffusion observed for metal electrodes evaporated on organic films.[81] The study of ultra-thin stacks could provide insights into the quantum charge transport across OSC/Gr vdW vertical heterostructures, besides potentially enabling FN tunneling at room temperature and therefore making possible the fabrication of organic flexible memories. The latter, which exploit FN tunneling to perform the write and erase operations, could be developed by stacking multiple C60/Gr interfaces.
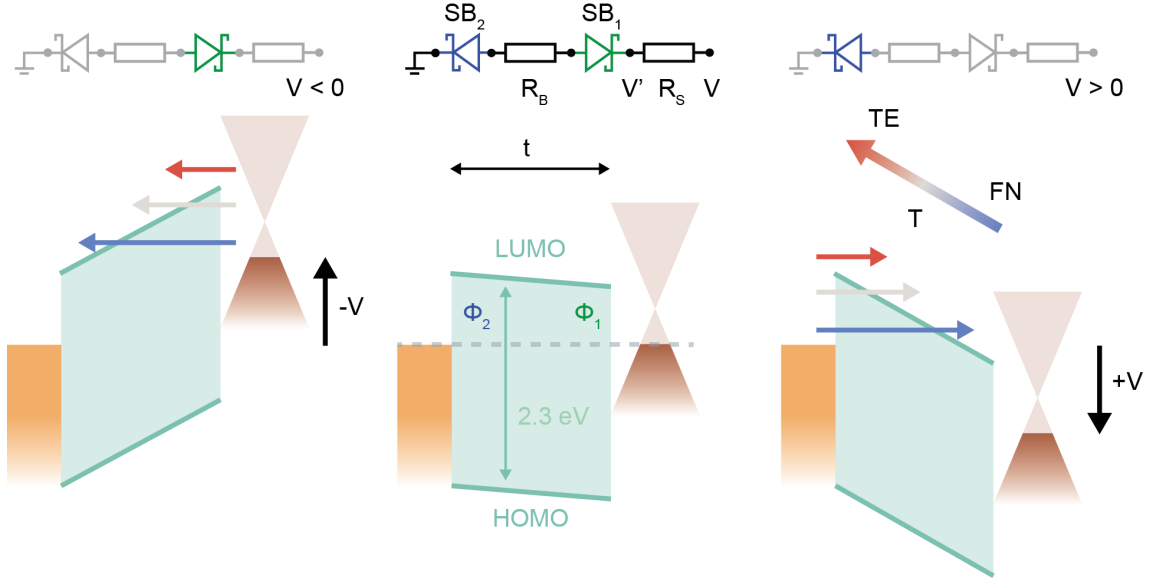
Figure 26: Equivalent electrical circuit model and energy band diagram of the vertical Au / C60 / Gr heterostructure. At $V = 0$, the system is at equilibrium and no current is flowing through the device. When $V < 0$, electrons are injected into the LUMO of the C60 from the graphene electrode. The total current is limited by the reverse current of the Schottky diode SB_1 of the circuit, which represent the Gr / C60 interface. When $V > 0$, electrons are injected into the LUMO of the C60 from the Au electrode. The total current is limited by the reverse current of the Schottky diode SB_2, which represent the Au / C60 interface. Contributions of the different injection mechanisms are represented by the colored arrows: FN tunneling is the dominant injection mechanism at low temperature and indicated by the blue arrow, while TE is the dominant injection mechanisms at high temperature and indicated by the red arrow. The grey arrow represent the intermediate regime, where the two contributions are comparable. In the equivalent circuit, R_S is the series resistance due to the graphene electrode and R_B is the bulk resistance of C60. Rs is ca. $20\,\text{k}\Omega$ at room temperature, as shown by the Graphene Bridge measurement in Appendix E (Fig. 53, Table 5), and therefore the voltage drop is negligible (i.e. $V' = V - R_S I \approx V$). The C60 is fully depleted and the voltage drops linearly over the entire structure.

Figure 26 shows the energy band diagram of the vertical Au / C60 / Gr hetetrostructure with the barrier heights extracted from the DSB model at room temperature (above $293\,\text{K}$) and confirmed by the FN model at low temperature (at $50\,\text{K}$). A small built-in potential of roughly $0.07\,\text{eV}$ is estimated from the difference between the potential barriers. Assuming that the LUMO and HOMO levels of C60 are located at $-4.1\,\text{eV}$ and $-6.4\,\text{eV}$, respectively, then: (i) the Fermi level of graphene is

located at ca. $E_F = E_{LUMO} - \Phi_{01} = -4.7\,\text{eV}$, which is possibly shifted with respect to the Dirac point due to p-doping induced by C60 and/or defects; and (ii) the Au work function is ca. $W = E_{LUMO} - \Phi_{02} = -4.8\,\text{eV}$, which is typically observed for Au surface with organic adsorbates, due to the pillow effect and/or interface states, which result in an interface dipole and possibly Fermi level pinning at the Au/OSC interface.[106, 165] It is worth observing that since the transport is injection limited, the thermal annealing has an observable effect on the energetics of the barrier: oxygen and moisture desorption affects the surface states, and thus possibly the Fermi level pinning, resulting in more or less conducting devices, as evinced by the I-V characteristics before and after annealing (Fig. 55).

7.3   Conclusion

This work describes the field- and thermal-induced charge transport mechanisms in Au / C60 / Gr VdW vertical heterostructures in the 50 K to 380 K temperature range. Devices having various nominal diameters, which ranges from from 5 µm to 50 µm, show the same electron transport characteristics. Thus, the fabrication of smaller devices is only limited by the lithography resolution and the fabrication process presented in this work.

Impedance analysis shows that C60 is fully depleted and thus that the voltage drops linearly over the entire structure. The static dielectric constant of C60 extracted from the geometrical capacitance is $\epsilon_r = 3.8$. The electrical transport measurements across the vertical heterostructure at high temperature (above 300 K) are well described by the DSB model, which gives $\Phi_{01} = (0.58\pm0.01)\,\mathrm{eV}$, $\Phi_{02} = (0.65\pm0.02)\,\mathrm{eV}$, $n_1 = 1.033 \pm 0.002$ and $n_2 = 1.036 \pm 0.003$ from the measurements at room temperature (293 K) at the Gr / C60 and Au / C60 interfaces, respectively. At low temperature (50 K), the measurements are well described by FN tunneling, which gives $\Phi_{01} = 0.54 \pm 0.07 eV$ and $\Phi_{02} = 0.60 \pm 0.05 eV$ for the Gr / C60 and Au / C60 interfaces. The energy barriers extracted from the two models are very similar. These findings reveal that the charge transport is injection-limited in the temperature range from 50 K to 380 K. The current is dominated by TE at high temperature (above 200 K) and limited by FN tunneling at low temperature (below 100 K). The charge transport at intermediate temperature (from room temperature down to 100 nm) is possibly described by a hybrid process where thermally excited charge carriers can tunnel through the potential barriers into the LUMO level of C60. From the electrical measurements, direct tunneling is predicted for thin C60 layers of maximum $\approx 4\,\mathrm{nm}$.

Finally, this study shows that CVD graphene can be used as a top electrode in C60 thin film vertical devices. The fabrication process can potentially be applied to other multilayer hybrid van der Waals heterostructures where the charge transport across neat Gr / OSC interfaces define the functionality of the devices. For instance, tunneling mechanisms could be exploited in high frequency devices such as organic hot electron transistor, permeable-base transistors and organic flexible memories.

7.4   Experimetal Methods

Materials

C60 (99.9%) powder was purchased from Sigma-Aldrich and evaporated without further treatments. CVD graphene was grown on copper foils using an in-house automated setup and following the growth protocol that can be found elsewhere.[83, 141, 142]

Fabrication

Devices were fabricated on a Si(525 µm) / SiO$_2$(335 nm) substrate by photolithography and under ambient conditions, as described in Appendix E. The chip includes two distinct groups of devices: (i) 119 Au / C60 / Gr Vertical Stacks (refer to Figure 23a for a schematic of the device structure) and (ii) 34 Graphene Bridges (refer to Appendix E Fig. 52). The chip overview is given in Appendix E (Table 64). In both Vertical Stacks and Graphene Bridges, the C60 thin film is interposed between a bottom gold and a top graphene circular electrodes. In the Graphene Bridge architecture, graphene is laterally contacted in order to measure its resistance (see Appendix E for the electrical scheme). The chip includes devices having graphene electrodes of various nominal diameter, i.e. 5, 10, 15, 20, 25, 30 and 50 µm, while the Au bottom electrodes are 2 µm larger. In short, Au electrodes were pre-patterned and deposited by e-beam physical vapour deposition (EBPVD) and lift-off. Then, the C60 thin film was thermally evaporated ($\approx 0.2\,\text{Ås}^{-1}$, 1×10^{-6} mbar) and patterned by lift-off. Finally, the graphene sheet was wet transferred on the chip and patterned into the top electrode circular shape by Reactive ion etching (RIE).

Electrical characterization

The electrical measurements were performed under various conditions, i.e.in air, at room temperature in dark, under vacuum ($\approx 1 \times 10^{-6}$ mbar) in dark, using the Semiconductor Parameter Analyzer Keithley 4200. The I-V characteristics of the Vertical Stacks were measured in the $-10\,\text{V}$ to $10\,\text{V}$ voltage range, with sweep rate of ca. $1\,\text{Vs}^{-1}$, steps of $50\,\text{mV}$ and internal averaging of $20\,\text{mV}$. The Au electrode was connected to ground. The graphene resistance was measured in Graphene Bridge devices by sweeping the voltage in the $-50\,\text{mV}$ to $50\,\text{mV}$ voltage range, with sweep rate of ca. $20\,\text{mVs}^{-1}$, steps of $1\,\text{mV}$ and internal averaging of $20\,\text{ms}$.
The temperature-dependent I-Vs were measured in the $50\,\text{K}$ - $285\,\text{K}$ temperature range, in steps of $5\,\text{K}$, using a Lakeshore probe station (CRX-6.5K), under vacuum ($\approx 1 \times 10^{-6}$ mbar) and in dark. The electronics consisted of an AdWin Gold II ADC-DAC and a Femto DDPCA-300 current to voltage converter. Matlab scripts were

used for the data acquisition. The I-V characteristics of the Vertical Stacks were measured in the $-10\,\mathrm{V}$ to $10\,\mathrm{V}$ voltage range, with sweep rate of ca. $150\,\mathrm{mVs^{-1}}$, steps of $10\,\mathrm{mV}$ and with internal averaging of $60\,\mathrm{ms}$. For the charge transport analysis, the backward and forward I-V sweeps for positive and negative biases were considered, respectively. The full I-V sweeps (forward and backward) for representative devices measured at room temperature ($293\,\mathrm{K}$) and at low temperature ($50\,\mathrm{K}$) can be found in the Appendix E (Fig. 63). An Agilent 4294a Precision Impedance Analyzer was used to measure the impedance of 3 representative devices per area. Python scripts were used to control the instrument. The measurement was performed in dark, under vacuum ($1 \times 10^{-6}\,\mathrm{mbar}$) and the oscillator level was set to $100\,\mathrm{mV}$ in the in the $40\,\mathrm{Hz}$ - $1\,\mathrm{MHz}$ frequency range, 201 data points were acquired. The open/short compensation method was applied to the measurements after the data acquisition and following the Agilent impedance measurement handbook.[49] Devices for the open/short compensation were embedded on the chip for this scope.

Raman spectroscopy

The WITec Alpha 300R confocal Raman microscope was used with a LD 100x objective (Zeiss EC Epiplan-Neofluar Dic, NA = 0.75) and a $300\,\mathrm{mm}$ lens-based spectrometer (grating: $600\,\mathrm{gmm^{-1}}$). Raman spectra were collected with a $532\,\mathrm{nm}$ excitation wavelength under ambient conditions. The laser power and integration time of $0.1\,\mathrm{mW}$ and $120\,\mathrm{s}$ were set for the device, while graphene spectrum on SiO_2 was acquired using a laser power and integration time of $1\,\mathrm{mW}$ and $60\,\mathrm{s}$.

Atomic force microscopy (AFM)

The height image was measured under ambient conditions using a Bruker Icon AFM in tapping mode. The AFM was equipped with a TESPA-V2 cantilever with a tip apex radius of $7\,\mathrm{nm}$, with a resonant frequency $320\,\mathrm{kHz}$ and a spring constant of $37\,\mathrm{Nm^{-1}}$.

FIB-SEM

The cross-section of the representative device was prepared using a FEI Helios 660 G3 UC FIB/SEM system. To protect the graphene and semiconductor layers from damage during the cutting process, a layer of Platinum was deposited in two steps: first through electron-induced deposition ($3\,\mathrm{keV}$, $800\,\mathrm{pA}$) and then through ion-induced deposition ($30\,\mathrm{keV}$, $230\,\mathrm{pA}$). The cross-section was then cut in a $30\,\mathrm{kV}$ gallium ion beam at an ion current of $47\,\mathrm{nA}$. After cutting, the cross-section was polished in sequential steps, decreasing the ion current down to a minimum of $790\,\mathrm{pA}$.

Modeling, fitting and plotting

Python scripts were developed for the modeling, fitting and visualization of the data. The main libraries that were implemented are: (i) scipy curve_fit,[126] for the FN modeling and for the extraction of the graphene resistance (ii) lmfit[176] Model for the DSB modeling (iii) impedance.py[143] for the impedance spectroscopy analyis.

8   Towards Vertical Organic Graphene Base Transistors

In this final section, we present the concept, the working principle and possible applications of a novel organic transistor, the Vertical Organic Graphene Base Transisor (VOGBT), which can possibly exploit the electronic properties of the graphene-organic interfaces investigated in this work.
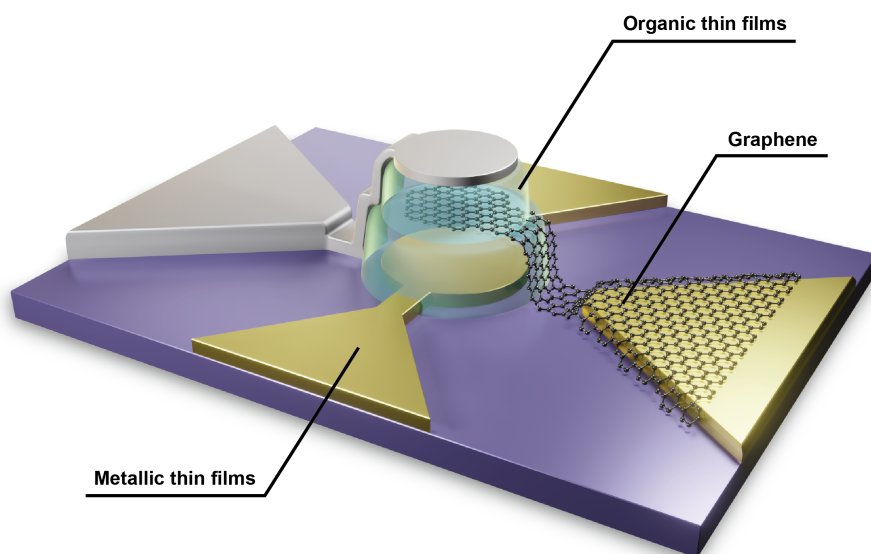
Abstract

The Vertical Organic Permeable Base Transisor (VOPBT) architecture is very promising to overcome the limitations of conventional OTFTs, which are typically operating at low frequencies and high voltages. In recent years, the device geometry and the fabrication processes of the VOPBT have been optimized to implement thin insulated and porous metallic films, thus, increasing the charge carriers permeability of the base electrodes. In this work, we propose to use graphene as an alternative to the conventional metallic base electrode in VOPBT. We first review the working principles and performance metrics of the device, which are based on the electrical properties of the Gr/OSC interfaces studies in our previous works. Then, we discuss how graphene, with its ultimate thinness and high conductivity, can enable the fabrication of organic transistors with superior operational frequency and high current gain. The potential challenges and limitations set by the device geometry, contact resistances, quantum capacitance of graphene and the charge mobility of the OSCs layers are introduced. Finally, we propose a possible fabrication approach for the VOGBT and we discuss its integration into organic optoelectronic devices.

8.1   Introduction

The concept of Permeable-Base Transistor (PBT) was proposed more than 50 years ago,[177,178] and demonstrated for the first time by Crowell and Sze in 1967.[179] Similar to the vacuum tube triodes configuration, the structure of this inorganic solid-state PBT was made of a gold grid embedded between two silicon semiconductors. The presence of a Schottky barrier between silicon and the gold electrode allowed the modulation of the current flow through the vertical semiconductor channels by adjusting the applied voltage on the grid. Two conditions were identified to ensure that the current would cross the base electrode: (i) the metal base must be thinner than the carrier mean free path of the metal to allow ballistic transport through the base, i.e less than few tens of nanometers at room temperature for most conductive metals;[180] and/or (ii) pinholes must be lithographically induced in the metal base to form a grid,[181] avoiding the screening of the electrical field applied from the emitter to the collector electrode and allowing carriers to cross the base. The potential of the PBT lies in its ability to operate at low voltage and high frequency, as well as its high integration density attributed to its vertical structure.[182,183] After the first demonstration by Crowell and Sze,[179] several inorganic PBT that were fabricated using different technologies have been reported. For instance, the growth of GaAs by Chemical Vapour Deposition (CVD) on tungsten grid,[182] and of silicon by molecular beam epitaxy on $CoSi_2$.[181,184] Although the devices demonstrated a promising high current density at low voltage and simulations predicted operation frequencies up to hundred of GHz,[183] the low current gain and the difficulty to integrate the PBTs with conventional CMOS technologies have represented major challenges for the development of applications.[181,184,185] However, in more recent years the permeable-base architecture was proposed to overcome the limitations of the planar Organic Thin Film Transistor (OTFT), e.g. low transconductance, low cut-off frequency and low integration.[57,67,80] In fact, the short emitter-collector distance of typically few hunred of nanometers, which is given by the thickness of the OSCs, allows high frequency operation at low voltage, in contrast to the the longer channel of the planar OTFT which is typically tens to hundreds of micrometers. These permeable base devices implemented a metal base electrode sandwiched between various OSCs suchs as C60,[66,73,74] Pentacene,[74,186] copper phthalocyanine[187] and poly-hexyl tertiophene.[188] The VOPBTs with nanoporous aluminium base electrodes have been finely optimised to reach the record transition frequency of 40 MHz in a pulse-biasing mode at $V_{CE} = 8.6$ V, rectification ratio larger than 1×10^8 and current density of $1\,kA/cm^2$.[56,61,63,66] Instead of the porous metallic electrode, we propose to use graphene as a premable-base in VOPBT. According to our previ-

ous results, the formation of Shottky barriers at the Gr/OSC interfaces combined with the ultra-thin graphene base electrode will enable the fabrication of the Vertical Organic Graphene Base Transisor (VOGBT). From the other specific properties of graphene, including high electrical conductivity and low electrostatic screening, we can expect increasing the current gain and frequency response of the VOPBT. However, to the best of our knowledge, no results have been published yet on the implementation of graphene as permable-base in VOPBT devices. In the following paragraphs, supported by our prior findings, we outline what we believe are the main steps and challenges for the realization of such a device.

8.2   Working principle
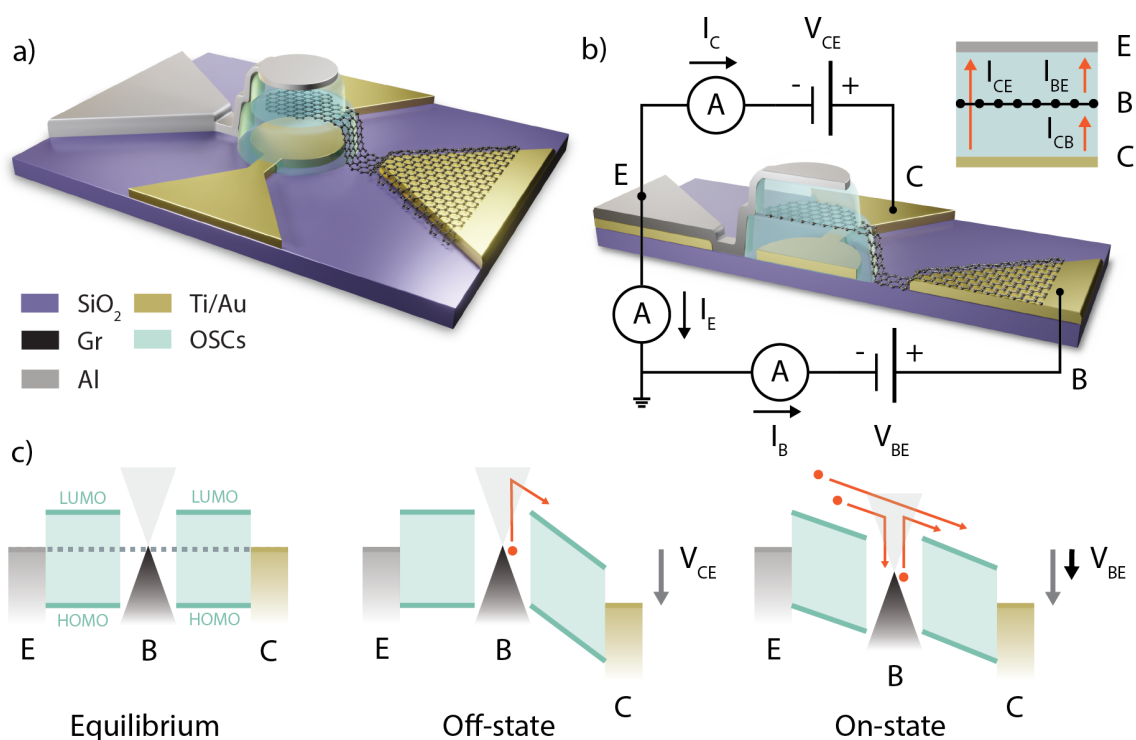
Figure 27:   (a) 3D schematic of a *n*-type Vertical Organic Graphene Base Transisor (VOGBT). (b) Section of the VOGBT illustrating the applied voltages and measured currents in the common emitter configuration. The inset shows the internal currents, which are not directly measurable. (c) Energy diagram of an *n*-type VOGBT showing the equilibrium condition, the on-state and the off-state of the transistor.

Figures 27a-b show the 3D schematic of a *n*-type VOGBT on a Si/SiO$_2$ substrate, its cross-section and electrical scheme. In this common emitter configuration, three parallel electrode are separated by two Organic Semiconductors (OSCs). Electric

charges are injected from the upper metal contact, i.e. the emitter (E), and enter the nearby organic semiconductor (OSC). They then traverse the permeable graphene electrode, i.e. the base (B), and the second OSC before being collected by the lower metal contact, i.e. the collector (C). The amount of charges collected by the base will depend on the electrical potential applied to it, while some charges will be emitted from the base and injected into the collector. Figure 27b shows the electrical currents I_E, I_C and I_B measured at the three terminals of the device. It is useful to express these external currents as functions of the internal currents I_{CE}, I_{CB} and I_{BE}, which are showed on the inset of Figure 27b and cannot be directly measured. In formula,

$$I_E = I_{CE} + I_{BE} \tag{11}$$

$$I_B = I_{BE} - I_{CB} \tag{12}$$

$$I_C = I_{CE} + I_{CB} \tag{13}$$

A deeper comprehension of these relationships can be gained through the examination of the energy diagram presented in Figure 27c. Under equilibrium conditions, all three electrodes are grounded, resulting in the absence of current flow within the device. In the off-state, a voltage V_{CE} is applied to the collector, enabling the thermal emission of charges from the base electrode to the adjacent Organic Semiconductor (OSC), which subsequently reach the collector. Since the base and emitter electrodes are at the same voltage level, no current I_{BE} is expected. However, the large Schottky barrier at the Gr/OSC interface will result in a small base-collector current $I_{CB} \approx 0$ (reverse-biased diode current). In the on-state, in addition to the bias V_{CE}, a voltage V_{BE} is applied to the base electrode. While the thermionic emission current I_{CB} is reduced, the emitter-collector current I_{CE} is established by the charges that are injected at the emitter and subsequently tunnel across the thin graphene base electrode. Therefore, the transmission of charges through the base can be modulated by the potential at the graphene electrode, thus affecting the charge injected at the emitter and arriving at the collector. Accordingly, the operation of the VOGBT would only be possible due to the low electrostatic screening of graphene and the ability of the charge carriers to tunnel through the thin graphene base, in contrast to the VOPBT where the charge carriers cross the nanometer pinholes of the metallic base. Nevertheless, some charges will scatter nearby the graphene region and relax into the base, resulting in the current I_{BE}. It is worth noticing that Ohmic contact at the emitter is necessary to obtain high-current den-

sity. Assuming that the base leakage I_{CB} is small compared to the collector current I_C, the transmittance α and current gain β of the device can be defined in terms of external currents as follows:[189]

$$\alpha = \frac{I_{CE}}{I_E} = \frac{I_C - I_{CB}}{I_E} \approx \frac{I_C}{I_E} \tag{14}$$

$$\beta = \frac{I_{CE}}{I_{BE}} = \frac{I_C - I_{CB}}{I_B + I_{CB}} \approx \frac{I_C}{I_B} \tag{15}$$

It is possible to show that α, with $0 \leq \alpha \leq 1$, and β are related by the expression $\beta = \alpha/(1-\alpha)$,[189] and thus that a transmittance close to one ($\alpha \approx 1$) is necessary to obtain a high current gain. Device simulations showed that the base current I_B is not needed to operate the VOPBT,[61] where the base leakage is considered a pure parasitic effect. However, this may not hold true for the graphene base transistor, where the base is not perforated and charges will have to tunnel through the graphene base. Thus, while the working principles are similar to the VOPBT, whether the base current is needed to operate the VOGBT or not still have to be demonstrated. Another important performance metric of the device is the transconductance g_m, which is defined as the ratio of the change in the output current (dI_C) to the change in the base voltage (dV_{BE}) at a specific bias voltage (V_{CE}) of the transistor:

$$g_m = \left. \frac{dI_C}{dV_{BE}} \right|_{V_{CE}=const} \tag{16}$$

Transconductance is a crucial parameter in VOPBT for several reasons: (i) it determines the current gain of the transistor, which is essential for amplification; (ii) a high transconductance value allows the transistor to achieve amplification with lower power consumption, which is particularly important in low-power and portable electronic devices; (iii) transconductance influences the speed at which the transistor can switch between the on and off states. A higher transconductance generally means faster switching speeds, which is beneficial in high-frequency applications. While prior device simulations suggest the possibility of reaching frequencies within the gigahertz range,[72] in the following paragraphs, we address the problem through a simplified circuit analysis. In fact, the time response of the transistor, i.e. $\tau \approx RC$, can be typically estimated from its equivalent circuit model. In this regard, the DC and small-signal circuit of the VOGBT can be modeled as shown in Figure 28.
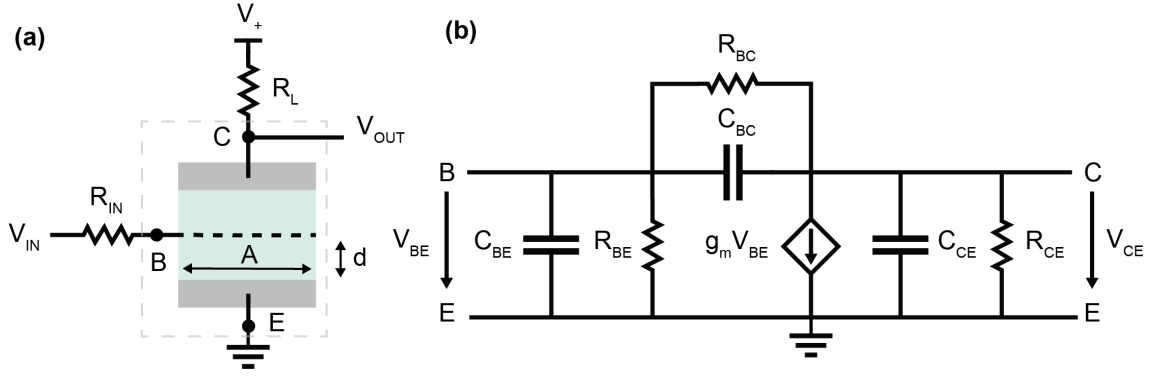
Figure 28:   Circuit analysis of the VOGBT. (a) Common-emitter configuration. R_{IN} is the input resistance and R_L is the load resistance. (b) Small-signal model. The capacitances defined by the graphene base and the outer electrodes are C_{BE} and C_{BC}, while the geometrical capacitance C_G given by the emitter and collector metal electrodes is C_{CE}. The OSCs are considered fully depleted (no modulation of the depletion region) and for thick OSCs layers, the quantum capacitance C_Q of graphene is neglected $A/C_{BE,BC} = 1/C_G + 1/C_Q \approx 1/C_G$. R_{BE} and R_{BC} represent the base leakage currents. R_{CE} is the bulk resistance of the OSCs and g_m is the low-frequency transconductance. The model assumes Ohmic contacts between the OSC and the metal at the emitter and collector electrodes.

Figure 28a shows the common-emitter configuration of the VOGBT, where the emitter terminal is grounded and used as the common terminal between the input V_{IN} and the output V_{OUT}. This is the most important configuration since the circuit can amplify the input signal. The input resistance R_{IN} represent the in-plane resistance of the metal and Gr lines interconnected to the base electrode, while R_L is the load resistance connected in series to the collector of the VOGBT. Here, the capacitance due to the metal interconnects C_{IN} is negligible compared to that of the overlapping electrodes of the device. However, in combination with R_{IN} it can limit the frequency response of the system, as we have already shown on our previous study on GFETs complementary inverters (Chapter 5). Thus, the device geometry should be optimized to reduce the contact resistance of the Gr/Metal interface, which is typically in the $200\,\Omega$ - $1\,k\Omega$ (Chapter 4) and reduce the in-plane graphene resistance, which is typically in the $5\,k\Omega$ - $100\,k\Omega$ for planar channels (Chapter 4) and in vertical stacks (Chapters 6 and 7). In this case, the use of graphene as 2D base electrode is advantageous because its high mobility is not significantly affected by the deposition of the organic molecules and therefore its relatively low in-plane resistance is preserved, as we have previously shown (Chapters 4, 6 and 7). Figure 28b shows the small-signal model of the VOGBT in the common emitter configuration. The trans-

fer characteristic of the device is modeled by a voltage-controlled current-source, where the low-frequency transconductance g_m can be derived from the DC measurements using Eq. 16. The resistances R_{BE} and R_{BC} represent the base leakage currents, that originate from the Schottky barriers at the Gr/OSC interfaces. The capacitor C_{BE}, C_{BC} (F) can be modeled by their geometrical capacitance C_G (F/m^2) in series with graphene's quantum capacitance C_Q (similar to GFET, see Chapter 4), while C_{CE} (F) is the geometrical capacitance given by the overlapping emitter and collector metal electrodes. It is important to note that the quantum capacitance C_Q (F/m^2) of graphene should also be considered in the electrical scheme of Figure 28b. The non-zero minimum of graphene's quantum capacitance at room temperature is predicted to be $C_{Q,min} \approx 0.8\,\mu\mathrm{Fcm}^{-2}$.[190] The devices quantum capacitance however is also influenced by the impurities and defects which typically results in a quantum capacitance much greater than the predicted value.[190] According to the geometrical capacitances measured in Chapter 7, the parallel plates capacitance per unit area is $C_G \approx \epsilon_0 \epsilon_r / t \approx 0.03\,\mu\mathrm{Fcm}^{-2}$, with $\epsilon_r = 3.8$ and $t = 100\,\mathrm{nm}$, which is much smaller than the quantum capacitance. Since the total capacitance can be modeled as two capacitor in series, and $C_G \ll C_Q$, the quantum capacitance can be neglected:

$$\frac{A}{C_{BE,BC}} = \frac{1}{C_G} + \frac{1}{C_Q} \approx \frac{1}{C_G} \tag{17}$$

As as a results, the capacitances C_{BE}, C_{BC} are only defined by the area A of the graphene electrode and the distance t between the electrodes, i.e. $C = \epsilon_0 \epsilon_r A / t$, where ϵ_r is the dielectric constant of the OSC (Chapters 6 and 7), as shown in Figure 28a. The capacitors C_{BE} and C_{BC} will charge (or discharge) through the resistance R_{IN} until the voltage at the base reaches V_{BE}. Taking the typical values of $R_{IN} = 10\,\mathrm{k\Omega}$ and $C_{BE} = 100\,\mathrm{fF}$, the capacitors will take approximately $\tau_i \approx R_{IN} C_{BE} \approx 1\,\mathrm{ns}$ to charge up. Thus, the frequency response of the device can be improved either by optimizing the lateral contact to graphene (reducing R_{IN}) or, by decreasing the device area and/or increasing the distance between the electrodes (reducing C_{BE}). Further simplifying, the output resistance is $R_{CE} \approx \rho t / A$, where ρ is the bulk resistivity of the OSCs, while the geometrical capacitance is $C_{CE} \approx \epsilon A / t$. As a result, the time constant $\tau_o \approx R_{CE} C_{CE} \approx \epsilon / \sigma$ solely depends on the material properties of the OSCs, i.e. the dielectric constant ϵ and the conductivity $\sigma \approx ne\mu$, where n is the charge carrier density, e is the elementary charge and μ is the charge carrier mobility. We can thus determine whether the the time response is limited by the intrinsic delay due to the OSCs charge mobility and carrier density or by

the geometry of the device. Taking $\epsilon_r = 3$, $n = 1 \times 10^{15}\,\mathrm{cm}^{-2}$ and $\mu = 10\,\mathrm{cm^2/Vs}$, the time constant is $\tau_o \approx 0.2\,\mathrm{ns}$. This confirms that frequency response in the GHz regime can be achieved using OSCs with a relatively high charge mobility. Figure 29a-b show the time constant as a function of the device area and thickness, respectively.
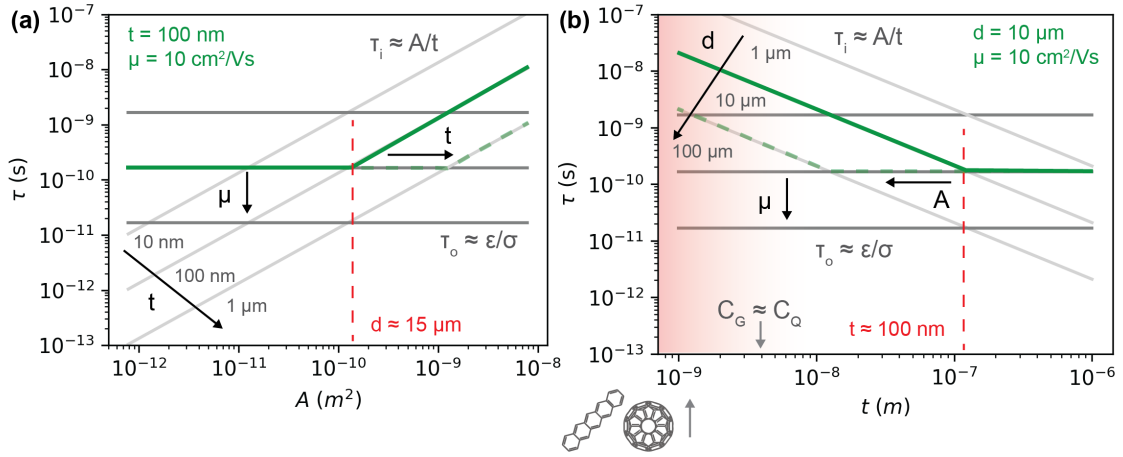
Figure 29:   Time constants τ_i and τ_o vs. device area $A = \pi d^2/4$ and thickness t. (a) τ vs. A for a fixed thickness $t = 100\,\mathrm{nm}$. (b) τ vs. t for a fixed area with diameter $d = 10\,\mathrm{\mu m}$. The red shaded area indicates where the OSC layer approaches the monolayer to sub-monolayer thickness, and where the circuit model reaches its limits. The graph also shows the OSC film thickness ($t \approx 5\,\mathrm{nm}$) which results in a geometrical capacitance comparable to the quantum capacitance of C_Q and that cannot be neglected.

Figure 29a shows that the frequency response is ultimately limited by the intrinsic properties of the OSC. As a results, the intrinsic delay can only be reduced by developing and implementing high-mobility semiconductors. On one hand, the device thickness can be reduced to few monolayers to achieve higher degrees of crystallinity and mobility (see red area in Fig. 29b), although different behaviors that cannot be simply expressed by a circuit model are also to be expected when approaching the molecular scale. On the other hand, a thick OSC layer is more likely to display a reduced charge carrier mobility, since the deposition of thick layers with long-range cristallinity also require precise control. However, large single crystal exhibiting in-plane FET mobilities up to $40\,\mathrm{cm^2/Vs}$, such as rubrene crystals, have already been grown.[191, 192] Another important aspect is the device geometry, this needs to be carefully designed in order to be able to drive the transistor at its maximum frequency. For instance, the device area cannot have a diameter larger than $15\,\mathrm{\mu m}$ for a $100\,\mathrm{nm}$ thick thin film. A larger area would result in a larger capacitance C_{BE},

and thus a slower response, as shown in Figure 29a. Alternatively a device with a diameter of $10\,\mu m$ should be thicker than $100\,nm$, as shown in 29b. In conclusion, implementing graphene can increase the transconductance g_m of the transistor thanks to an increased transmittance ratio α due the ultimate thinness of the base electrode. In addition, we have shown that the presence of large Schottky barrier in the range of 0.3 - 0.6 eV at the Gr/OSC interfaces (Chapters 6 7) can limit the base leakage I_B, and thus further increase the current gain β while reducing the power consumption. We have shown that the fabrication of devices with a frequency response in $100\,MHz$ - $1\,GHz$ range is feasible by keeping reasonable lateral size (tens of microns) and thickness of devices (hundred of nanomaeters) which can be implemented in cost-effective fabrication workflows. Although the $100\,MHz$ - $1\,GHz$ bandwidth may already meet the needs of most applications in flexible electronics, scaling down the dimensions of the devices can enable higher operational frequencies, at the cost of more complex and expensive fabrication techniques. Overall, we have discussed how the implementation of graphene as permable-base can ideally improve the performances of VOPBT. Nevertheless, to demonstrate a fully functional device, several steps need to be undertaken, which includes addressing fabrication issues like introducing doped layers between the emitter and the intrinsic OSC to optimize the charge injection, depositing the second OSC layer and patterning the metal electrode on top of the whole stack. Taking this into account, in the following paragraph we propose a possible fabrication approach for the VOGBT.

8.3 Fabrication approach

Here, we propose a general step by step approach, which is based on our previous results, that can be followed and adapted to fabricate the VOGBT. Figure 30a shows a photograph of the chip containing a set of 187 pre-pattened electrodes. The greyscale optical microscope picture (Figure 30b) shows the bottom metal electrodes. The different layers of the VOGBT, i.e. metal, graphene and intrinsic-OSC (i-OSC), are represented by different colors. The first step consists in depositing the first i-OSC layer, which is needed to lower the contact resistance at the injecting electrode, on top of the metal electrode (Fig. 30c). This can be achieved by thermal evaporation of small molecules or spin coating of polymers. For instance, it was shown that $W_2(hpp)_4$-doped C60 could be used between a Cr electrode and the intrinsic C60 layer.[73, 193, 194] However, it is essential to avoid exposure to air, which can lead to metal oxidation and degradation of the OSC-dopant, preventing the formation of an ohmic contact. Bearing this in mind, it can be challenging to fabricate a device that combines photolithography techniques to pattern graphene, which are typically

conducted in ambient environments, with the deposition techniques of organic semi-conductors that are generally carried out in inert atmospheres. The deposition (Fig. 30d) and patterning of the intrinsic and doped OSC could be done using lithography methods or evaporation through metallic masks, as we have already implemented to fabricate vertical Au-Pentacene-Al diodes in Appendix F. Large area CVD graphene can be deposited on the OSC layer (Fig. 30e) using the wet transfer method, showed in Chapters 6 and 7, or using other dry techniques such as lamination.[195] Then, a well defined graphene electrode can be realized by photolithography and RIE. With a particular focus on uniformity, a thin film of i-OSC should be deposited and patterned on top of graphene (Fig. 30f). Indeed, the morphology of the film deposited on graphene can vary depending on the specific molecules, as we have previously shown for C60 and Pentacene (Chapter 4). Finally, the top metallic electrode can by thermally evaporated through metal masks (as shown for Aluminum on Pentacene, Appendix) or patterned by photolithography.
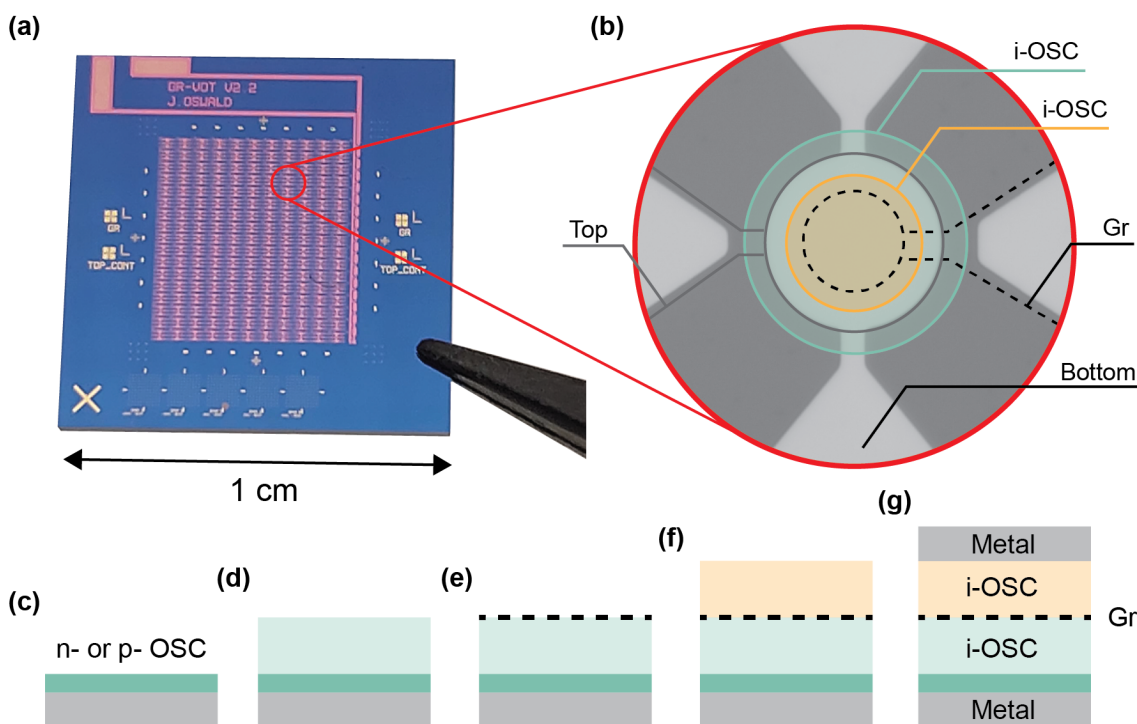
Figure 30:   Fabrication approach of the VOGBT. (a) Photograph of the chip with pre-patterned electrodes for a total of 187 devices. (b) Optical microscope image of the device electrodes. The colored regions indicate the target position of the different layers of the stack. The stacking steps (c-g) follow the same color code. (c) Deposition of the thin *n*- or *p*-doped OSC layer to ensure ohmic contact with the bottom electrode. (d) Deposition of the lower intrinsic OSC film. (e) Transfer and patterning of graphene. (f) Deposition of the upper intrinsic OSC layer. (g) Deposition of the top metal electrode.

8.4   Optoelectronic applications
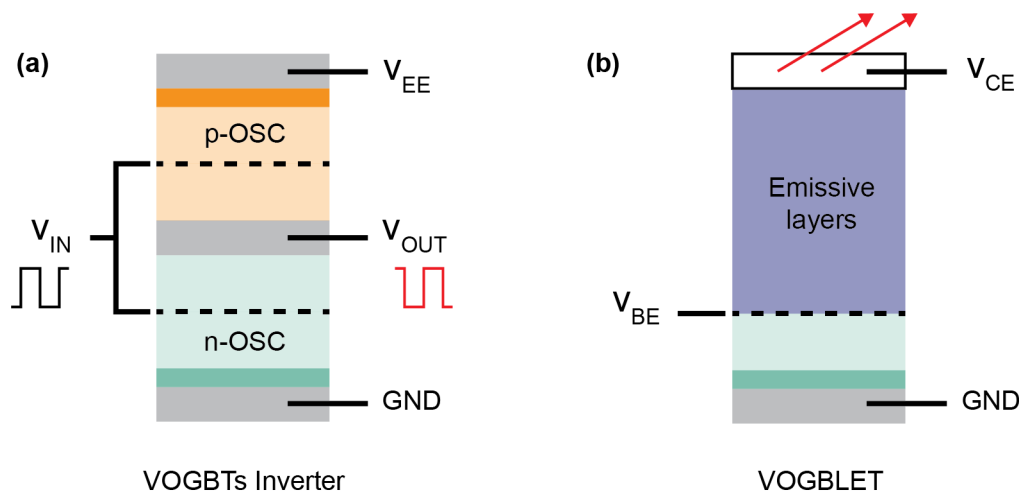
Figure 31:   (a) Cross-section and electrical scheme of a vertical complementary inverter using two VOGBTs. This architecture can be exploited to achieve higher levels of integration. (b) Cross-section and electrical scheme of a Vertical Organic Permable Base Light Emitting Transistor (VOPBLET) implementing graphene. The high-conductivity, flexibility and optical transparency of graphene can be beneficial for the development of flexible and high resolution-displays.

Vertical Organic Permeable Base Transisor (VOPBT) hold great promise for various applications, including amplifiers, inverters, ring oscillators, and control of OLEDs.[70,74,75] The vertical architecture and operational characteristics of these devices make them well-suited for these applications. In complementary inverters, n- and p-type transistors can be vertically stacked to achieve higher levels of integration, as illustrated in Figure 31a for two VOGBTs. Although ring oscillators based on vertical-channel dual-base transistors have been shown,[74] and other complex organic multilayered structures have been fabricated,[70] the integration of two VOPBTs into one vertical complementary inverter remains to be demonstrated. Furthermore, the high-conductivity, flexibility and optical transparency of graphene can be beneficial for the development of flexible and high resolution-displays. In particular, VOGBT can be used to efficiently control OLEDs by integrating them into the backplane of the displays, as illustrated in Figure 31b. A similar device has already been shown using an aluminium base to fabricate a Vertical Organic Permable Base Light Emitting Transistor (VOPBLET).[70] In this context, it is worth noticing that the properties of graphene, i.e. conductivity and optical transparency, make it also a good electrode material to contact light emitting layers.

9   Conclusion and outlook

In this research work, we have investigated the electrical properties of graphene-organic interfaces for electronic devices applications such as the graphene complementary inverter or the Vertical Organic Permeable Base Transisor (VOPBT). In particular, we focused on the charge transport in CVD graphene and across vertical graphene-organic interfaces. In our studies, we have used different techniques to fabricate devices made of graphene and organic semiconductors, such as the thermal evaporation of small molecules of C60 and Pentacene, and the solution-processed polymer P3HT. Overall, this dissertation can be subdivided in three major parts.

In the first part, we explored the effects of C60 and Pentacene molecules on the in-plane charge transport in CVD graphene. For this purpose, thin films of C60 and Pentacene were thermally evaporated on two separate chips including several GFETs. The morphology of the resulting Gr/C60 and Gr/Pentacene heterostructures was characterized by AFM. While we observed a uniform C60 film on graphene, the Pentacene film formed 3D elongated island on graphene. In both cases, the structure of the graphene channel was clearly distinguishable from the organic thin films deposited on top. In addition, we were able to reveal the coexistence of graphene and the small molecules by using Raman spectroscopy. From the electrical transfer characteristic of the GFETs, we deduced that C60 induces a downshift of the Fermi energy in graphene, while Pentacene induces a Fermi energy upshift. We thus demonstrated that n- and p-type behavior can be induced in CVD graphene by thermal evaporation of thin films of Pentacene and C60, respectively, without significantly affecting the charge mobility in graphene. Furthermore, we have exploited this knowledge to assemble complementary inverters based on C60 and Pentacene doped GFETs. The transfer characteristic of the devices demonstrated limited voltage swing and gain, while the dynamic response showed stable and well-defined logic levels up to 10 kHz. Nevertheless, our circuit simulations showed that by integrating the GFETs and carefully design the chip metal interconnects, it should be possible to fabricate a functional complementary inverter operating in the GHz frequency regime. Further studies on the relationship between the electrical conduction in the Gr/OSC heterostructures and the molecular organization may be relevant to optimize the charge transfer occurring at the Gr/OSC interfaces and meet the requirements of specific applications. Indeed, small molecules like Pentacene can either standup right or lie flat on graphene,[84] and correlating the field-effect transistors measurements to other non-destructive techniques can lead to a better understanding of the charge transfer at the Gr/OSC interface and thus of the electrical conduction in doped CVD graphene. For instance, Conductive Atomic Force

Microscopy (CAFM) and/or Kelvin Probe Force Microscopy (KPFM) can be used to investigate and correlate the topography, current and surface potential across the Gr/OSC heterostructures. Another possible future project involves the integration and encapsulation of the complementary inverter based on C60 and Pentacene doped CVD graphene. Here, the reduction of the gate insulator thickness and the optimization of the metal interconnects should be pursued to achieve a voltage gain greater than unity, thus matching the input and output logic levels and allowing to cascade the inverters in more complex circuits such as the ring oscillator. It is worth noticing that the devices presented in this work were fabricated on rigid substrates and characterized under vacuum. However, demonstrating the inverter characteristic on polymeric substrates remains a key milestone to achieve functional devices for applications in flexible electronics. The major challenges are represented by the transfer of CVD graphene on polymeric substrates and the encapsulation of the doped devices under controlled atmosphere, which is necessary to achieve air stability. In fact, preliminary studies on hBN encapsulation under ambient conditions showed that the transfer characteristics of the GFETs are lost (Appendix C, Fig. 41).

In the second part, we investigated the charge transport across vertical Au-OSC-Gr stacks. For this purpose, we developed a fabrication process based on photolithography that was compatible with the wet transfer of CVD graphene and with the deposition of the organic semiconductors. Thin films of the n-type small molecules of C60 and of the p-type polymer P3HT were chosen for the semiconducting layers. The former was deposited by thermal evaporation under vacuum, while the latter was solution-processed in ambient conditions. The OSCs layers were patterned by lift-off before the wet transfer and subsequent RIE patterning of the CVD graphene into the top electrode. We used AFM and Raman spectroscopy to show that the fabrication techniques were compatible with graphene and organic materials. From the impedance analysis, it was not only possible to extrapolate the dielectric constants of the semiconductors, but also to determine that the OSCs were fully depleted and thus that the voltage drops linearly over the entire structures. The current vs voltage (IV) traces for both OSCs showed a non-linear characteristic and a strong temperature dependence compatible with the termionic emission (TE) model. Furthermore, we implemented the Double Schottky Barrier (DSB) model to extrapolate from the IVs the energy barriers at the interfaces. Schottky barriers of about $0.3\,\mathrm{eV}$ and $0.6\,\mathrm{eV}$ were found at the Gr/P3HT and Gr/C60 interfaces, respectively. Therefore, the electrical currents in the two stacks are limited by the holes injection from the graphene electrode to P3HT, and by the electrons injection from the graphene

electrode to C60. These results demonstrate that graphene cannot be used to efficiently inject charges into intrinsic C60 and P3HT layers and thus that graphene could be implemented as a semi-permeable base electrode in n- and p-type VOPBT, where the base leakage current needs to be minimized to achieve good performances in terms of gain. However, similar energy barriers were found at the Au electrode where Ohmic contacts are required to (i) provide high current gain, and (ii) allow high frequency operation of the device. In order to address this requirement, future work should focus on the possible doping approaches for organic semiconductors.[11] Ohmic contact can be achieved by selecting the right metal electrode and introducing a doped OSC between the electrode and the intrinsic OSC. For example, F4TCNQ-doped P3HT layer can be placed between the Au electrode and the intrinsic P3HT layer,[196–198] while $W_2(hpp)_4$-doped C60 could be used between a Cr electrode and the intrinsic C60 layer.[73,193,194] The main challenge will be implementing the doping process and ensure its compatibility with the current fabrication process of the stacks. As a result, the IV characteristic of the doped devices should be similar to the single Schottky diode characteristic with a high rectification ratio (see for example the Au-Pentacene-Al diodes of Appendix F). Future work should also focus on reducing the OSC thickness, since the time delay of the VOPBT can be minimized by optimizing the lateral dimensions and reducing the thickness of the semiconducting layers, and in particular the thickness of the emitter OSC.[72] In this case, graphene can be transferred on top of the OSC without diffusing in the adjacent layer, in contrast to commonly evaporated metal electrodes,[81] enabling further reduction of the OSC thickness and potentially approaching the moelcular scale.

In the third part, we introduced the theory, operational mechanism, and potential applications of VOGBT that could take advantage of the electronic properties of the Gr/OSC interfaces examined in this research. Our GFETs investigations indicate that molecular doping of CVD graphene does not significantly influence the in-plane mobility of charge carriers, thereby facilitating the application and fast modulation of the base voltage through the lateral graphene electrode. Moreover, the formation of a Schottky barrier at the Gr/OSC, which will limit the base leakage current allowing high current gain, indicates that graphene could be a strong contender for a semi-permeable base electrode. Furthermore, as the ultimate thin base electrode, graphene should not only posses a higher transmittance ratio but also enables fast switching due to its high charge mobility, thereby augmenting its effectiveness and application in organic flexible electronics. This highlights the promising potential of graphene-organic interfaces for further research and development in VOGBT.

Nevertheless, to demonstrate a fully functional device, several steps need to be undertaken, which includes addressing issues like the deposition of the second OSC layer and the top metal electrode. While the OSC could also be thermally evaporated, the deposition and subsequent patterning of the metal electrode on top of the stack remain challenging. Specifically, extra caution should be exercised to prevent the potential problem of metal diffusion into the adjacent OSC layers, which could compromise the overall device performance and reliability. A possible solution to this challenge could be the utilization of graphene as the top electrode. Following a similar procedure used for the base electrode, a second sheet of graphene could be transferred and patterned by RIE on top of the stack. This approach could provide a neat interface at the top contact, while reducing the risk of undesired short circuits and maintaining the intrinsic properties of the device. Other issues like high base leakage could possibly be mitigated through encapsulation in insulating 2D materials such as hBN. Finally, it is crucial to electrically evaluate these devices, with their performance metrics such as current gain and frequency response, set against the standards of the most efficient organic transistors. This benchmarking step will provide a clear perspective on the device effectiveness and potential for practical applications.

In conclusion, new advances in the techniques for the growth of large-area graphene and transfer onto organic substrates will pave the way for novel applications exploiting the unique properties of hybrid graphene-organic materials. In this regard, the results presented in this work highlight the many challenges ahead for the fabrication of graphene-organic based heterostructures but also show their great potential for the development of flexible electronic devices that could work at high frequencies, such as the VOGBT.

References

[1] Kim, C.-H. & Kymissis, I. Graphene–organic hybrid electronics. *J. Mater. Chem. C* **5**, 4598–4613 (2017). URL `http://xlink.rsc.org/?DOI=C7TC00664K`.

[2] Lee, G.-H. *et al.* Heterostructures based on inorganic and organic van der Waals systems. *APL Materials* **2**, 092511 (2014). URL `http://aip.scitation.org/doi/10.1063/1.4894435`.

[3] Jariwala, D., Marks, T. J. & Hersam, M. C. Mixed-dimensional van der Waals heterostructures. *Nature Materials* **16**, 170–181 (2017). URL `http://www.nature.com/articles/nmat4703`.

[4] Gobbi, M., Orgiu, E. & Samorì, P. When 2D Materials Meet Molecules: Opportunities and Challenges of Hybrid Organic/Inorganic van der Waals Heterostructures. *Advanced Materials* **30**, 1706103 (2018). URL `http://doi.wiley.com/10.1002/adma.201706103`.

[5] Schlierf, A., Samorì, P. & Palermo, V. Graphene–organic composites for electronics: optical and electronic interactions in vacuum, liquids and thin solid films. *Journal of Materials Chemistry C* **2**, 3129 (2014). URL `http://xlink.rsc.org/?DOI=c3tc32153c`.

[6] Novoselov, K. S. *et al.* A roadmap for graphene. *Nature* **490**, 192–200 (2012). URL `https://www.nature.com/articles/nature11458`.

[7] Castro Neto, A. H., Guinea, F., Peres, N. M. R., Novoselov, K. S. & Geim, A. K. The electronic properties of graphene. *Reviews of Modern Physics* **81**, 109–162 (2009). URL `https://link.aps.org/doi/10.1103/RevModPhys.81.109`.

[8] Sang, M., Shin, J., Kim, K. & Yu, K. Electronic and Thermal Properties of Graphene and Recent Advances in Graphene Based Electronics Applications. *Nanomaterials* **9**, 374 (2019). URL `https://www.mdpi.com/2079-4991/9/3/374`.

[9] Avouris, P. Graphene: Electronic and Photonic Properties and Devices. *Nano Letters* **10**, 4285–4294 (2010). URL `https://pubs.acs.org/doi/10.1021/nl102824h`.

[10] Randviir, E. P., Brownson, D. A. & Banks, C. E. A decade of graphene research: production, applications and outlook. *Materials Today* **17**, 426–432 (2014). URL `https://linkinghub.elsevier.com/retrieve/pii/S1369702114002144`.

[11] Scaccabarozzi, A. D. *et al.* Doping Approaches for Organic Semiconductors. *Chemical Reviews* **122**, 4420–4492 (2022). URL `https://pubs.acs.org/doi/10.1021/acs.chemrev.1c00581`.

[12] Jiang, H. & Hu, W. The Emergence of Organic Single-Crystal Electronics. *Angewandte Chemie International Edition* **59**, 1408–1428 (2020). URL `https://onlinelibrary.wiley.com/doi/10.1002/anie.201814439`.

[13] Liu, K., Ouyang, B., Guo, X., Guo, Y. & Liu, Y. Advances in flexible organic field-effect transistors and their applications for flexible electronics. *npj Flexible Electronics* **6**, 1 (2022). URL `https://www.nature.com/articles/s41528-022-00133-3`.

[14] Hu, P., He, X. & Jiang, H. Greater than 10 cm2V-1s -1 : A breakthrough of organic semiconductors for field-effect transistors. *InfoMat* **3**, 613–630 (2021). URL `https://onlinelibrary.wiley.com/doi/10.1002/inf2.12188`.

[15] Sirringhaus, H. 25th Anniversary Article: Organic Field-Effect Transistors: The Path Beyond Amorphous Silicon. *Advanced Materials* **26**, 1319–1335 (2014). URL `https://onlinelibrary.wiley.com/doi/10.1002/adma.201304346`.

[16] Paterson, A. F. *et al.* Recent Progress in High-Mobility Organic Transistors: A Reality Check. *Advanced Materials* **30**, 1801079 (2018). URL `https://onlinelibrary.wiley.com/doi/10.1002/adma.201801079`.

[17] Baeg, K.-J., Caironi, M. & Noh, Y.-Y. Toward Printed Integrated Circuits based on Unipolar or Ambipolar Polymer Semiconductors. *Advanced Materials* **25**, 4210–4244 (2013). URL `https://onlinelibrary.wiley.com/doi/10.1002/adma.201205361`.

[18] Fukuda, K. *et al.* Fully-printed high-performance organic thin-film transistors and circuitry on one-micron-thick polymer films. *Nature Communications* **5**, 4147 (2014). URL `https://www.nature.com/articles/ncomms5147`.

[19] Scheunemann, D. *et al.* Charge transport in doped conjugated polymers for organic thermoelectrics. *Chemical Physics Reviews* **3**, 021309 (2022). URL `https://aip.scitation.org/doi/10.1063/5.0080820`.

[20] Yao, Y., Dong, H. & Hu, W. Charge Transport in Organic and Polymeric Semiconductors for Flexible and Stretchable Devices. *Advanced Materials* **28**, 4513–4523 (2016). URL `https://onlinelibrary.wiley.com/doi/10.1002/adma.201503007`.

[21] Chen, Y., Yao, Y., Turetta, N. & Samorì, P. Vertical organic transistors with short channels for multifunctional optoelectronic devices. *Journal of Materials Chemistry C* **10**, 2494–2506 (2022). URL `http://xlink.rsc.org/?DOI=D1TC05055A`.

[22] Ojeda-Aristizabal, C., Bao, W. & Fuhrer, M. S. Thin-film barristor: A gate-tunable vertical graphene-pentacene device. *Physical Review B* **88**, 035435 (2013). URL `https://link.aps.org/doi/10.1103/PhysRevB.88.035435`.

[23] He, D. *et al.* Two-dimensional quasi-freestanding molecular crystals for high-performance organic field-effect transistors. *Nature Communications* **5**, 5162 (2014). URL `https://www.nature.com/articles/ncomms6162`.

[24] Hlaing, H. *et al.* Low-Voltage Organic Electronics Based on a Gate-Tunable Injection Barrier in Vertical graphene-organic Semiconductor Heterostructures. *Nano Letters* **15**, 69–74 (2015). URL `https://pubs.acs.org/doi/10.1021/nl5029599`.

[25] Parui, S. *et al.* Gate-Controlled Energy Barrier at a Graphene/Molecular Semiconductor Junction. *Advanced Functional Materials* **25**, 2972–2979 (2015). URL `https://onlinelibrary.wiley.com/doi/10.1002/adfm.201403407`.

[26] Yang, H. *et al.* Graphene Barristor, a Triode Device with a Gate-Controlled Schottky Barrier. *Science* **336**, 1140–1143 (2012). URL `https://www.science.org/doi/10.1126/science.1220527`.

[27] Novoselov, K. S. *et al.* Electric Field Effect in Atomically Thin Carbon Films. *Science* **306**, 666–669 (2004). URL `https://www.science.org/doi/10.1126/science.1102896`.

[28] Butler, S. Z. *et al.* Progress, Challenges, and Opportunities in Two-Dimensional Materials Beyond Graphene. *ACS Nano* **7**, 2898–2926 (2013). URL `https://pubs.acs.org/doi/10.1021/nn400280c`.

[29] Fiori, G. *et al.* Electronics based on two-dimensional materials. *Nature Nanotechnology* **9**, 768–779 (2014). URL `https://www.nature.com/articles/nnano.2014.207`.

[30] Wang, Q. H., Kalantar-Zadeh, K., Kis, A., Coleman, J. N. & Strano, M. S. Electronics and optoelectronics of two-dimensional transition metal dichalcogenides. *Nature Nanotechnology* **7**, 699–712 (2012). URL `https://www.nature.com/articles/nnano.2012.193`.

[31] As thin as it gets. *Nature Materials* **16**, 155–155 (2017). URL `https://www.nature.com/articles/nmat4854`.

[32] Mounet, N. *et al.* Two-dimensional materials from high-throughput computational exfoliation of experimentally known compounds. *Nature Nanotechnology* **13**, 246–252 (2018). URL `https://www.nature.com/articles/s41565-017-0035-5`.

[33] Geim, A. K. & Grigorieva, I. V. Van der Waals heterostructures. *Nature* **499**, 419–425 (2013). URL `https://www.nature.com/articles/nature12385`.

[34] Lee, G.-H. *et al.* Heterostructures based on inorganic and organic van der Waals systems. *APL Materials* **2**, 092511 (2014). URL `https://pubs.aip.org/apm/article/2/9/092511/150606/Heterostructures-based-on-inorganic-and-organic`.

[35] Liu, Y. *et al.* Van der Waals heterostructures and devices. *Nature Reviews Materials* **1**, 16042 (2016). URL `https://www.nature.com/articles/natrevmats201642`.

[36] Novoselov, K. S., Mishchenko, A., Carvalho, A. & Castro Neto, A. H. 2D materials and van der Waals heterostructures. *Science* **353**, aac9439 (2016). URL `https://www.science.org/doi/10.1126/science.aac9439`.

[37] Huang, M. *et al.* Multifunctional high-performance van der Waals heterostructures. *Nature Nanotechnology* **12**, 1148–1154 (2017). URL `https://www.nature.com/articles/nnano.2017.208`.

[38] Akinwande, D. *et al.* A review on mechanics and mechanical properties of 2D materials—Graphene and beyond. *Extreme Mechanics Letters* **13**, 42–77 (2017). URL `https://linkinghub.elsevier.com/retrieve/pii/S235243161630236X`.

[39] Schwierz, F. Graphene transistors. *Nature Nanotechnology* **5**, 487–496 (2010). URL `http://www.nature.com/articles/nnano.2010.89`.

[40] Wu, Y. *et al.* High-frequency, scaled graphene transistors on diamond-like carbon. *Nature* **472**, 74–78 (2011). URL `https://www.nature.com/articles/nature09979`.

[41] Schwierz, F. Graphene Transistors: Status, Prospects, and Problems. *Proceedings of the IEEE* **101**, 1567–1584 (2013). URL `http://ieeexplore.ieee.org/document/6518205/`.

[42] Schwierz, F., Pezoldt, J. & Granzner, R. Two-dimensional materials and their prospects in transistor electronics. *Nanoscale* **7**, 8261–8283 (2015). URL `http://xlink.rsc.org/?DOI=C5NR01052G`.

[43] Traversi, F., Russo, V. & Sordan, R. Integrated complementary graphene inverter. *Applied Physics Letters* **94**, 223312 (2009). URL `https://pubs.aip.org/aip/apl/article/336918`.

[44] Rizzi, L. G. *et al.* Cascading Wafer-Scale Integrated Graphene Complementary Inverters under Ambient Conditions. *Nano Letters* **12**, 3948–3953 (2012). URL `https://pubs.acs.org/doi/10.1021/nl301079r`.

[45] Yu, W. J. *et al.* Vertically stacked multi-heterostructures of layered materials for logic transistors and complementary inverters. *Nature Materials* **12**, 246–252 (2013). URL `https://www.nature.com/articles/nmat3518`.

[46] Kang, J. *et al.* Probing Out-of-Plane Charge Transport in Black Phosphorus with Graphene-Contacted Vertical Field-Effect Transistors. *Nano Letters* **16**, 2580–2585 (2016). URL `https://pubs.acs.org/doi/10.1021/acs.nanolett.6b00144`.

[47] Georgiou, T. *et al.* Vertical field-effect transistor based on graphene–WS2 heterostructures for flexible and transparent electronics. *Nature Nanotechnology* **8**, 100–103 (2013). URL `https://www.nature.com/articles/nnano.2012.224`.

[48] Sarker, B. K. & Khondaker, S. I. Thermionic Emission and Tunneling at Carbon Nanotube–Organic Semiconductor Interface. *ACS Nano* **6**, 4993–4999 (2012). URL `https://pubs.acs.org/doi/10.1021/nn300544v`.

[49] Shim, J. *et al.* Extremely Large Gate Modulation in Vertical Graphene/WSe $_2$ Heterojunction Barristor Based on a Novel Transport Mechanism. *Advanced Materials* **28**, 5293–5299 (2016). URL `https://onlinelibrary.wiley.com/doi/10.1002/adma.201506004`.

[50] Di Bartolomeo, A. Graphene Schottky diodes: An experimental review of the rectifying graphene/semiconductor heterojunction. *Physics Reports* **606**, 1–58 (2016). URL `https://linkinghub.elsevier.com/retrieve/pii/S0370157315004354`.

[51] Berke, K. *et al.* Current transport across the pentacene/CVD-grown graphene interface for diode applications. *Journal of Physics: Condensed Matter* **24**, 255802 (2012). URL `https://iopscience.iop.org/article/10.1088/0953-8984/24/25/255802`.

[52] Lemaitre, M. G. *et al.* Improved Transfer of Graphene for Gated Schottky-Junction, Vertical, Organic, Field-Effect Transistors. *ACS Nano* **6**, 9095–9102 (2012). URL `https://pubs.acs.org/doi/10.1021/nn303848k`.

[53] Wang, Q. H. & Hersam, M. C. Room-temperature molecular-resolution characterization of self-assembled organic monolayers on epitaxial graphene. *Nature Chemistry* **1**, 206–211 (2009). URL `https://www.nature.com/articles/nchem.212`.

[54] Singha Roy, S., Bindl, D. J. & Arnold, M. S. Templating Highly Crystalline Organic Semiconductors Using Atomic Membranes of Graphene at the Anode/Organic Interface. *The Journal of Physical Chemistry Letters* **3**, 873–878 (2012). URL `https://pubs.acs.org/doi/10.1021/jz201559g`.

[55] Kim, K. *et al.* Structural and Electrical Investigation of C60–Graphene Vertical Heterostructures. *ACS Nano* **9**, 5922–5928 (2015). URL `https://doi.org/10.1021/acsnano.5b00581`. Publisher: American Chemical Society.

[56] Klinger, M. P. *et al.* Advanced Organic Permeable-Base Transistor with Superior Performance. *Advanced Materials* **27**, 7734–7739 (2015). URL `http://doi.wiley.com/10.1002/adma.201502788`.

[57] Nawaz, A., Merces, L., Ferro, L. M. M., Sonar, P. & Bufon, C. C. B. Impact of Planar and Vertical Organic Field-Effect Transistors on Flexible Electronics. *Advanced Materials* **35**, 2204804 (2023). URL `https://onlinelibrary.wiley.com/doi/abs/10.1002/adma.202204804`. _eprint: https://onlinelibrary.wiley.com/doi/pdf/10.1002/adma.202204804.

58 Liu, J. *et al.* Vertical Organic Field-Effect Transistors. *Advanced Functional Materials* **29**, 1808453 (2019). URL `https://onlinelibrary.wiley.com/doi/10.1002/adfm.201808453`.

59 Dahal, D., Paudel, P. R., Kaphle, V., Radha Krishnan, R. K. & Lüssem, B. Influence of Injection Barrier on Vertical Organic Field Effect Transistors. *ACS Applied Materials & Interfaces* **14**, 7063–7072 (2022). URL `https://pubs.acs.org/doi/10.1021/acsami.1c20382`.

60 Lim, K. *et al.* Anodization for Simplified Processing and Efficient Charge Transport in Vertical Organic Field-Effect Transistors. *Advanced Functional Materials* **30**, 2001703 (2020). URL `https://onlinelibrary.wiley.com/doi/10.1002/adfm.202001703`.

61 Guo, E., Dollinger, F., Amaya, B., Fischer, A. & Kleemann, H. Organic Permeable Base Transistors – Insights and Perspectives. *Advanced Optical Materials* 2002058 (2021). URL `https://onlinelibrary.wiley.com/doi/10.1002/adom.202002058`.

62 Al-Shadeedi, A., Liu, S., Kaphle, V., Keum, C.-M. & Lüssem, B. Scaling of High-Performance Organic Permeable Base Transistors. *Advanced Electronic Materials* **5**, 1800728 (2019). URL `http://doi.wiley.com/10.1002/aelm.201800728`.

63 Dollinger, F. *et al.* Electrically Stable Organic Permeable Base Transistors for Display Applications. *Advanced Electronic Materials* **5**, 1900576 (2019). URL `https://onlinelibrary.wiley.com/doi/abs/10.1002/aelm.201900576`.

64 Darbandy, G. *et al.* Unraveling Structure and Device Operation of Organic Permeable Base Transistors. *Advanced Electronic Materials* **6**, 2000230 (2020). URL `https://onlinelibrary.wiley.com/doi/10.1002/aelm.202000230`.

65 Al-shadeedi, A. *et al.* Modeling tunnel currents in organic permeable-base transistors. *Synthetic Metals* **252**, 82–90 (2019). URL `https://linkinghub.elsevier.com/retrieve/pii/S0379677919301183`.

66 Klinger, M. P. *et al.* Organic Power Electronics: Transistor Operation in the kA/cm2 Regime. *Scientific Reports* **7**, 44713 (2017). URL `http://www.nature.com/articles/srep44713`.

67 Kleemann, H., Günther, A. A., Leo, K. & Lüssem, B. High-Performance Vertical Organic Transistors. *Small* **9**, 3670–3677 (2013). URL `https://onlinelibrary.wiley.com/doi/10.1002/smll.201202321`.

68 Subedi, K. N., Al-Shadeedi, A. & Lüssem, B. Stability of organic permeable base transistors. *Applied Physics Letters* **115**, 193301 (2019). URL `http://aip.scitation.org/doi/10.1063/1.5125233`.

69 Kaschura, F. *et al.* Operation mechanism of high performance organic permeable base transistors with an insulated and perforated base electrode. *Journal of Applied Physics* **120**, 094501 (2016). URL `http://aip.scitation.org/doi/10.1063/1.4962009`.

70 Wu, Z. *et al.* Efficient and low-voltage vertical organic permeable base light-emitting transistors. *Nature Materials* **20**, 1007–1014 (2021). URL `http://www.nature.com/articles/s41563-021-00937-0`.

71 Agrawal, K., Rana, O., Singh, N., Srivastava, R. & Rajput, S. S. Low voltage organic permeable base N-type transistor. *Applied Physics Letters* **109**, 163301 (2016). URL `http://aip.scitation.org/doi/10.1063/1.4964838`.

References

[72] Chen, W., So, F. & Guo, J. Intrinsic delay of permeable base transistor. *Journal of Applied Physics* **116**, 044505 (2014). URL `http://aip.scitation.org/doi/10.1063/1.4891231`.

[73] Fischer, A., Scholz, R., Leo, K. & Lüssem, B. An all C60 vertical transistor for high frequency and high current density applications. *Applied Physics Letters* **101**, 213303 (2012). URL `http://aip.scitation.org/doi/10.1063/1.4767391`.

[74] Guo, E. *et al.* Integrated complementary inverters and ring oscillators based on vertical-channel dual-base organic thin-film transistors. *Nature Electronics* (2021). URL `http://www.nature.com/articles/s41928-021-00613-w`.

[75] Huang, W. & Facchetti, A. Organic circuits reach new heights. *Nature Electronics* (2021). URL `https://www.nature.com/articles/s41928-021-00634-5`.

[76] Fischer, A., Siebeneicher, P., Kleemann, H., Leo, K. & Lüssem, B. Bidirectional operation of vertical organic triodes. *Journal of Applied Physics* **111**, 044507 (2012). URL `http://aip.scitation.org/doi/10.1063/1.3686744`.

[77] Wang, S.-J. *et al.* Organic bipolar transistors. *Nature* **606**, 700–705 (2022). URL `https://www.nature.com/articles/s41586-022-04837-4`.

[78] Höppner, M. *et al.* High-Frequency Operation of Vertical Organic Field-Effect Transistors. *Advanced Science* **9**, 2201660 (2022). URL `https://onlinelibrary.wiley.com/doi/10.1002/advs.202201660`.

[79] Kheradmand-Boroujeni, B. *et al.* A Pulse-Biasing Small-Signal Measurement Technique Enabling 40 MHz Operation of Vertical Organic Transistors. *Scientific Reports* **8**, 7643 (2018). URL `https://www.nature.com/articles/s41598-018-26008-0`.

[80] Kleemann, H., Krechan, K., Fischer, A. & Leo, K. A Review of Vertical Organic Transistors. *Advanced Functional Materials* **30**, 1907113 (2020). URL `https://onlinelibrary.wiley.com/doi/abs/10.1002/adfm.201907113`. _eprint: https://onlinelibrary.wiley.com/doi/pdf/10.1002/adfm.201907113.

[81] Zhang, G. *et al.* Extensive Penetration of Evaporated Electrode Metals into Fullerene Films: Intercalated Metal Nanostructures and Influence on Device Architecture. *ACS Applied Materials & Interfaces* **7**, 25247–25258 (2015). URL `https://pubs.acs.org/doi/10.1021/acsami.5b06944`.

[82] Oswald, J. *et al.* Charge Transport Across Au–P3HT–Graphene van der Waals Vertical Heterostructures. *ACS Applied Materials & Interfaces* acsami.2c13148 (2022). URL `https://pubs.acs.org/doi/10.1021/acsami.2c13148`.

[83] Schmuck, O., Beretta, D., Furrer, R., Oswald, J. & Calame, M. A method to fabricate nanoscale gaps in graphene nano-constrictions by electrical breakdown. *AIP Advances* **12**, 055312 (2022). URL `https://aip.scitation.org/doi/10.1063/5.0087564`.

[84] Daher Mansour, M. *et al.* Nanoscale electronic transport at graphene/pentacene van der Waals interfaces. *Nanoscale* 10.1039.D2NR06682C (2023). URL `http://xlink.rsc.org/?DOI=D2NR06682C`.

[85] Oswald, J. *et al.* The Effect of C60 and Pentacene Adsorbates on the Electrical Properties of CVD Graphene on SiO2. *Nanomaterials* **13**, 1134 (2023). URL `https://www.mdpi.com/2079-4991/13/6/1134`.

[86] Huet, B., Raskin, J.-P., Snyder, D. W. & Redwing, J. M. Fundamental limitations in transferred CVD graphene caused by Cu catalyst surface morphology. *Carbon* **163**, 95–104 (2020). URL `https://linkinghub.elsevier.com/retrieve/pii/S0008622320302220`.

[87] Hempel, M. *et al.* Repeated roll-to-roll transfer of two-dimensional materials by electrochemical delamination. *Nanoscale* **10**, 5522–5531 (2018). URL `http://xlink.rsc.org/?DOI=C7NR07369K`.

[88] Wu, Z. T. *et al.* The influence of chemical solvents on the properties of CVD graphene: Influence of chemical solvents on properties of CVD graphene. *Journal of Raman Spectroscopy* **46**, 21–24 (2015). URL `https://onlinelibrary.wiley.com/doi/10.1002/jrs.4582`.

[89] *Agilent Impedance Measurement Handbook* (Agilent Technologies, 2009), 4th edition edn.

[90] Huisman, E. H. *et al.* High Gain Hybrid Graphene–Organic Semiconductor Phototransistors. *ACS Applied Materials & Interfaces* **7**, 11083–11088 (2015). URL `https://pubs.acs.org/doi/10.1021/acsami.5b00610`.

[91] Shangguan, Q. *et al.* Design of Ultra-Narrow Band Graphene Refractive Index Sensor. *Sensors* **22**, 6483 (2022). URL `https://www.mdpi.com/1424-8220/22/17/6483`.

[92] Garg, R., Elmas, S., Nann, T. & Andersson, M. R. Deposition Methods of Graphene as Electrode Material for Organic Solar Cells. *Advanced Energy Materials* **7**, 1601393 (2017). URL `https://onlinelibrary.wiley.com/doi/10.1002/aenm.201601393`.

[93] Adetayo, A. E., Ahmed, T. N., Zakhidov, A. & Beall, G. W. Improvements of Organic Light-Emitting Diodes Using Graphene as an Emerging and Efficient Transparent Conducting Electrode Material. *Advanced Optical Materials* **9**, 2002102 (2021). URL `https://onlinelibrary.wiley.com/doi/abs/10.1002/adom.202002102`. _eprint: https://onlinelibrary.wiley.com/doi/pdf/10.1002/adom.202002102.

[94] Liu, L., Liu, Y. & Duan, X. Graphene-based vertical thin film transistors. *Science China Information Sciences* **63**, 201401 (2020). URL `https://link.springer.com/10.1007/s11432-020-2806-8`.

[95] Liu, Y., Zhou, H., Weiss, N. O., Huang, Y. & Duan, X. High-Performance Organic Vertical Thin Film Transistor Using Graphene as a Tunable Contact. *ACS Nano* **9**, 11102–11108 (2015). URL `https://pubs.acs.org/doi/10.1021/acsnano.5b04612`.

[96] Parui, S. *et al.* Graphene as an electrode for solution-processed electron-transporting organic transistors. *Nanoscale* **9**, 10178–10185 (2017). URL `http://xlink.rsc.org/?DOI=C7NR01007A`.

[97] Shih, C.-J. *et al.* Partially-Screened Field Effect and Selective Carrier Injection at Organic Semiconductor/Graphene Heterointerface. *Nano Lett.* 9 (2015).

[98] Chhikara, M. *et al.* Pentacene on graphene: Differences between single layer and bilayer. *Carbon* **69**, 162–168 (2014). URL `https://linkinghub.elsevier.com/retrieve/pii/S0008622313011445`.

[99] Lee, W. H. *et al.* Surface-Directed Molecular Assembly of Pentacene on Monolayer Graphene for High-Performance Organic Transistors. *Journal of the American Chemical Society* **133**, 4447–4454 (2011). URL `https://pubs.acs.org/doi/10.1021/ja1097463`.

References

[100] Chhikara, M., Pavlica, E., Matković, A., Gajić, R. & Bratina, G. Effect of Water Layer at the SiO $_2$ /Graphene Interface on Pentacene Morphology. *Langmuir* **30**, 11681–11688 (2014). URL https://pubs.acs.org/doi/10.1021/la502970q.

[101] Ojeda-Aristizabal, C. *et al.* Molecular Arrangement and Charge Transfer in C $_{60}$ /Graphene Heterostructures. *ACS Nano* **11**, 4686–4693 (2017). URL https://pubs.acs.org/doi/10.1021/acsnano.7b00551.

[102] Anthopoulos, T. D. *et al.* High performance n-channel organic field-effect transistors and ring oscillators based on C60 fullerene films. *Applied Physics Letters* **89**, 213504 (2006). URL http://aip.scitation.org/doi/10.1063/1.2387892.

[103] Klauk, H. *et al.* High-mobility polymer gate dielectric pentacene thin film transistors. *Journal of Applied Physics* **92**, 5259–5263 (2002). URL http://aip.scitation.org/doi/10.1063/1.1511826.

[104] Park, S. H. *et al.* The electronic structure of C60/ZnPc interface for organic photovoltaic device with blended layer architecture. *Applied Physics Letters* **96**, 013302 (2010). URL http://aip.scitation.org/doi/10.1063/1.3285174.

[105] Horowitz, G. Validity of the concept of band edge in organic semiconductors. *Journal of Applied Physics* **118**, 115502 (2015). URL http://aip.scitation.org/doi/10.1063/1.4931061.

[106] Hwang, J., Wan, A. & Kahn, A. Energetics of metal–organic interfaces: New experiments and assessment of the field. *Materials Science and Engineering: R: Reports* **64**, 1–31 (2009). URL https://linkinghub.elsevier.com/retrieve/pii/S0927796X08001228.

[107] Garg, R., Dutta, N. & Choudhury, N. Work Function Engineering of Graphene. *Nanomaterials* **4**, 267–300 (2014). URL http://www.mdpi.com/2079-4991/4/2/267.

[108] Yu, Y.-J. *et al.* Tuning the Graphene Work Function by Electric Field Effect. *Nano Letters* **9**, 3430–3434 (2009). URL https://pubs.acs.org/doi/10.1021/nl901572a.

[109] Long, F. *et al.* Characteristic Work Function Variations of Graphene Line Defects. *ACS Applied Materials & Interfaces* **8**, 18360–18366 (2016). URL https://pubs.acs.org/doi/10.1021/acsami.6b04853.

[110] Joshi, P., Romero, H. E., Neal, A. T., Toutam, V. K. & Tadigadapa, S. A. Intrinsic doping and gate hysteresis in graphene field effect devices fabricated on SiO $_2$ substrates. *Journal of Physics: Condensed Matter* **22**, 334214 (2010). URL https://iopscience.iop.org/article/10.1088/0953-8984/22/33/334214.

[111] Singh, A. K., Singh, A. K. & Sinha, S. R. P. Fermi-Level Modulation of Chemical Vapor Deposition-Grown Monolayer Graphene via Nanoparticles to Macromolecular Dopants. *ACS Omega* **7**, 744–751 (2022). URL https://pubs.acs.org/doi/10.1021/acsomega.1c05394.

[112] Lee, S. *et al.* Enhanced Charge Injection in Pentacene Field-Effect Transistors with Graphene Electrodes. *Advanced Materials* **23**, 100–105 (2011). URL https://onlinelibrary.wiley.com/doi/abs/10.1002/adma.201003165. _eprint: https://onlinelibrary.wiley.com/doi/pdf/10.1002/adma.201003165.

[113] Parker, J. H., Feldman, D. W. & Ashkin, M. Raman Scattering by Silicon and Germanium. *Physical Review* **155**, 712–714 (1967). URL https://link.aps.org/doi/10.1103/PhysRev.155.712.

[114] Kuzmany, H., Matus, M., Burger, B. & Winter, J. Raman Scattering in C60 fullerenes and fullerides. *Advanced Materials* **6**, 731–745 (1994). URL `https://onlinelibrary.wiley.com/doi/10.1002/adma.19940061004`.

[115] Parisse, P., Passacantando, M., Picozzi, S. & Ottaviano, L. Conductivity of the thin film phase of pentacene. *Organic Electronics* **7**, 403–409 (2006). URL `https://linkinghub.elsevier.com/retrieve/pii/S1566119906000814`.

[116] Shearer, C. J., Slattery, A. D., Stapleton, A. J., Shapter, J. G. & Gibson, C. T. Accurate thickness measurement of graphene. *Nanotechnology* **27**, 125704 (2016). URL `https://iopscience.iop.org/article/10.1088/0957-4484/27/12/125704`.

[117] Seto, K. & Furukawa, Y. Study on solid structure of pentacene thin films using Raman imaging: Study on solid structure of pentacene thin films using Raman imaging. *Journal of Raman Spectroscopy* **43**, 2015–2019 (2012). URL `https://onlinelibrary.wiley.com/doi/10.1002/jrs.4090`.

[118] Fang, T., Konar, A., Xing, H. & Jena, D. Carrier statistics and quantum capacitance of graphene sheets and ribbons. *Applied Physics Letters* **91**, 092109 (2007). URL `http://aip.scitation.org/doi/10.1063/1.2776887`.

[119] S. Muller, R. & I. Kamins, T. *Device Electronics for Integrated Circuits* (Wiley, 2022), 3 edn.

[120] Jnawali, G. *et al.* Observation of Ground- and Excited-State Charge Transfer at the C$_{60}$ /Graphene Interface. *ACS Nano* **9**, 7175–7185 (2015). URL `https://pubs.acs.org/doi/10.1021/acsnano.5b01896`.

[121] Chen, J.-H. *et al.* Charged-impurity scattering in graphene. *Nature Physics* **4**, 377–381 (2008). URL `http://www.nature.com/articles/nphys935`.

[122] Lee, S. *et al.* Dirac-Point Shift by Carrier Injection Barrier in Graphene Field-Effect Transistor Operation at Room Temperature. *ACS Applied Materials & Interfaces* **10**, 10618–10621 (2018). URL `https://pubs.acs.org/doi/10.1021/acsami.8b02294`.

[123] Lee, E. J. H., Balasubramanian, K., Weitz, R. T., Burghard, M. & Kern, K. Contact and edge effects in graphene devices. *Nature Nanotechnology* **3**, 486–490 (2008). URL `http://www.nature.com/articles/nnano.2008.172`.

[124] Harris, C. R. *et al.* Array programming with NumPy. *Nature* **585**, 357–362 (2020). URL `https://www.nature.com/articles/s41586-020-2649-2`.

[125] McKinney, W. Data Structures for Statistical Computing in Python. 56–61 (Austin, Texas, 2010). URL `https://conference.scipy.org/proceedings/scipy2010/mckinney.html`.

[126] Virtanen, P. *et al.* SciPy 1.0: fundamental algorithms for scientific computing in Python. *Nature Methods* **17**, 261–272 (2020). URL `http://www.nature.com/articles/s41592-019-0686-2`.

[127] Das, T., Sharma, B. K., Katiyar, A. K. & Ahn, J.-H. Graphene-based flexible and wearable electronics. *Journal of Semiconductors* **39**, 011007 (2018). URL `https://iopscience.iop.org/article/10.1088/1674-4926/39/1/011007`.

[128] Bahri, M. *et al.* Recent advances in chemical vapour deposition techniques for graphene-based nanoarchitectures: From synthesis to contemporary applications. *Coordination Chemistry Reviews* **475**, 214910 (2023). URL `https://www.sciencedirect.com/science/article/pii/S0010854522005057`.

[129] Banerjee, A. N. Green syntheses of graphene and its applications in internet of things (IoT)—a status review. *Nanotechnology* **33**, 322003 (2022). URL `https://iopscience.iop.org/article/10.1088/1361-6528/ac6599`.

[130] Du, J. *et al.* Advances in Flexible Optoelectronics Based on Chemical Vapor Deposition-Grown Graphene. *Advanced Functional Materials* **32**, 2203115 (2022). URL `https://onlinelibrary.wiley.com/doi/abs/10.1002/adfm.202203115`. _eprint: https://onlinelibrary.wiley.com/doi/pdf/10.1002/adfm.202203115.

[131] Lee, I.-Y. *et al.* Hydrazine-based n-type doping process to modulate Dirac point of graphene and its application to complementary inverter. *Organic Electronics* **14**, 1586–1590 (2013). URL `https://linkinghub.elsevier.com/retrieve/pii/S1566119913001365`.

[132] Oswald, J. *et al.* Field and Thermal Emission Limited Charge Injection in Au–C60–Graphene van der Waals Vertical Heterostructures for Organic Electronics. *ACS Applied Nano Materials* acsanm.3c01090 (2023). URL `https://pubs.acs.org/doi/10.1021/acsanm.3c01090`.

[133] Wang, Y., Tong, S. W., Xu, X. F., Özyilmaz, B. & Loh, K. P. Interface Engineering of Layer-by-Layer Stacked Graphene Anodes for High-Performance Organic Solar Cells. *Advanced Materials* **23**, 1514–1518 (2011). URL `https://onlinelibrary.wiley.com/doi/10.1002/adma.201003673`.

[134] Park, H., Rowehl, J. A., Kim, K. K., Bulovic, V. & Kong, J. Doped graphene electrodes for organic solar cells. *Nanotechnology* **21**, 505204 (2010). URL `https://iopscience.iop.org/article/10.1088/0957-4484/21/50/505204`.

[135] Liu, Z., Li, J. & Yan, F. Package-Free Flexible Organic Solar Cells with Graphene top Electrodes. *Advanced Materials* **25**, 4296–4301 (2013). URL `https://onlinelibrary.wiley.com/doi/10.1002/adma.201205337`.

[136] Grotevent, M. J. *et al.* Nanoprinted Quantum Dot–Graphene Photodetectors. *Advanced Optical Materials* **7**, 1900019 (2019). URL `https://onlinelibrary.wiley.com/doi/10.1002/adom.201900019`.

[137] Matyba, P., Yamaguchi, H., Chhowalla, M., Robinson, N. D. & Edman, L. Flexible and Metal-Free Light-Emitting Electrochemical Cells Based on Graphene and PEDOT-PSS as the Electrode Materials. *ACS Nano* **5**, 574–580 (2011). URL `https://pubs.acs.org/doi/10.1021/nn102704h`.

[138] Wu, J. *et al.* Organic Light-Emitting Diodes on Solution-Processed Graphene Transparent Electrodes. *ACS Nano* **4**, 43–48 (2010). URL `https://pubs.acs.org/doi/10.1021/nn900728d`.

[139] Lee, C.-H. *et al.* Atomically thin p–n junctions with van der Waals heterointerfaces. *Nature Nanotechnology* **9**, 676–681 (2014). URL `http://www.nature.com/articles/nnano.2014.150`.

[140] Pang, S., Hernandez, Y., Feng, X. & Müllen, K. Graphene as Transparent Electrode Material for Organic Electronics. *Advanced Materials* **23**, 2779–2795 (2011). URL `https://onlinelibrary.wiley.com/doi/10.1002/adma.201100304`.

[141] Braun, O. *et al.* Optimized graphene electrodes for contacting graphene nanoribbons. *Carbon* **184**, 331–339 (2021). URL `https://linkinghub.elsevier.com/retrieve/pii/S0008622321007934`.

[142] Braun, O. *et al.* Spatially mapping thermal transport in graphene by an opto-thermal method. *npj 2D Materials and Applications* **6**, 6 (2022). URL `https://www.nature.com/articles/s41699-021-00277-2`.

[143] Murbach, M., Gerwe, B., Dawson-Elli, N. & Tsui, L.-k. impedance.py: A Python package for electrochemical impedance analysis. *Journal of Open Source Software* **5**, 2349 (2020). URL `https://joss.theoj.org/papers/10.21105/joss.02349`.

[144] Tsoi, W. C. *et al.* The Nature of In-Plane Skeleton Raman Modes of P3HT and Their Correlation to the Degree of Molecular Order in P3HT:PCBM Blend Thin Films. *Journal of the American Chemical Society* **133**, 9834–9843 (2011). URL `https://pubs.acs.org/doi/10.1021/ja2013104`.

[145] Kumar, S. *et al.* Study of P3HT/ PCBM morphology using Raman spectroscopy. 100074 (Bikaner, India, 2018). URL `http://aip.scitation.org/doi/abs/10.1063/1.5033010`.

[146] Rao, C. N. R. & Sood, A. K. (eds.) *Graphene* (Wiley, 2012), 1 edn. URL `https://onlinelibrary.wiley.com/doi/book/10.1002/9783527651122`. 10.1002/9783527651122.

[147] Abdou, M. S. A., Orfino, F. P., Son, Y. & Holdcroft, S. Interaction of Oxygen with Conjugated Polymers: Charge Transfer Complex Formation with Poly(3-alkylthiophenes). *Journal of the American Chemical Society* **119**, 4518–4524 (1997). URL `https://pubs.acs.org/doi/10.1021/ja964229j`.

[148] Rep, D., Huisman, B.-H., Meijer, E., Prins, P. & Klapwijk, T. Charge-Transport in Partially-Ordered Regioregular Poly(3-Hexylthiophene) Studied as a Function of the Charge-carrier Density. *MRS Proceedings* **660**, JJ7.9 (2000). URL `http://link.springer.com/10.1557/PROC-660-JJ7.9`.

[149] Rep, D., Morpurgo, A. & Klapwijk, T. Doping-dependent charge injection into regioregular poly(3-hexylthiophene). *Organic Electronics* **4**, 201–207 (2003). URL `https://linkinghub.elsevier.com/retrieve/pii/S1566119903000168`.

[150] Sze, S. M. & Ng, K. K. *Physics of semiconductor devices* (Wiley-Interscience, Hoboken, N.J, 2007), 3rd ed edn.

[151] Zhong, H. *et al.* Charge transport mechanisms of graphene/semiconductor Schottky barriers: A theoretical and experimental study. *Journal of Applied Physics* **115**, 013701 (2014). URL `http://aip.scitation.org/doi/10.1063/1.4859500`.

[152] Knipper, M. *et al.* Impedance Spectroscopy on Polymer-Fullerene Solar Cells .

[153] Wang, C. *et al.* High Dielectric Constant Semiconducting Poly(3-alkylthiophene)s from Side Chain Modification with Polar Sulfinyl and Sulfonyl Groups. *Macromolecules* **51**, 9368–9381 (2018). URL `https://pubs.acs.org/doi/10.1021/acs.macromol.8b01895`.

[154] Shen, Y. & Gupta, M. C. Investigation of electrical characteristics of P3HT:PCBM organic solar cells. In *2012 38th IEEE Photovoltaic Specialists Conference*, 002770–002774 (IEEE, Austin, TX, USA, 2012). URL `http://ieeexplore.ieee.org/document/6318167/`.

[155] Scott, J. & Malliaras, G. G. Charge injection and recombination at the metal–organic interface. *Chemical Physics Letters* **299**, 115–119 (1999). URL `https://linkinghub.elsevier.com/retrieve/pii/S0009261498012779`.

[156] Scott, J. C. Metal–organic interface and charge injection in organic electronic devices. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* **21**, 521–531 (2003). URL http://avs.scitation.org/doi/10.1116/1.1559919.

[157] Lou, Y., Wang, Z., Naka, S. & Okada, H. Charge transport characteristics in P3HT:PCBM organic blends under illumination: Influence of metal work functions. *Chemical Physics Letters* **529**, 64–68 (2012). URL https://linkinghub.elsevier.com/retrieve/pii/S0009261412001194.

[158] Mott, N. F. & Gurney, R. W. *Electronic Processes in Ionic Crystals* (Oxford University Press, London, 1940).

[159] Tessler, N. Experimental techniques and the underlying device physics. *Journal of Polymer Science Part B: Polymer Physics* **52**, 1119–1152 (2014). URL https://onlinelibrary.wiley.com/doi/10.1002/polb.23550.

[160] Meijer, E. J., Mangnus, A. V. G., Hart, C. M., de Leeuw, D. M. & Klapwijk, T. M. Frequency behavior and the Mott–Schottky analysis in poly(3-hexyl thiophene) metal–insulator–semiconductor diodes. *Applied Physics Letters* **78**, 3902–3904 (2001). URL http://aip.scitation.org/doi/10.1063/1.1378803.

[161] Kim, C. H. *et al.* Capacitive behavior of pentacene-based diodes: Quasistatic dielectric constant and dielectric strength. *Journal of Applied Physics* **109**, 083710 (2011). URL http://aip.scitation.org/doi/10.1063/1.3574661.

[162] Melitz, W., Shen, J., Kummel, A. C. & Lee, S. Kelvin probe force microscopy and its application. *Surface Science Reports* **66**, 1–27 (2011). URL https://linkinghub.elsevier.com/retrieve/pii/S0167572910000841.

[163] Thakur, A. K., Mukherjee, A. K., Preethichandra, D. M. G., Takashima, W. & Kaneto, K. Charge injection mechanism across the Au-poly(3-hexylthiophene-2,5-diyl) interface. *Journal of Applied Physics* **101**, 104508 (2007). URL http://aip.scitation.org/doi/10.1063/1.2734955.

[164] Lyon, J. E. *et al.* Photoemission study of the poly(3-hexylthiophene)/Au interface. *Applied Physics Letters* **88**, 222109 (2006). URL http://aip.scitation.org/doi/10.1063/1.2208267.

[165] Braun, S., Salaneck, W. R. & Fahlman, M. Energy-Level Alignment at Organic/Metal and Organic/Organic Interfaces. *Advanced Materials* **21**, 1450–1472 (2009). URL http://doi.wiley.com/10.1002/adma.200802893.

[166] Li, X. *et al.* Transfer of Large-Area Graphene Films for High-Performance Transparent Conductive Electrodes. *Nano Letters* **9**, 4359–4363 (2009). URL https://pubs.acs.org/doi/10.1021/nl902623y.

[167] Petrone, N. *et al.* Flexible Graphene Field-Effect Transistors Encapsulated in Hexagonal Boron Nitride. *ACS Nano* **9**, 8953–8959 (2015). URL https://pubs.acs.org/doi/10.1021/acsnano.5b02816.

[168] Kim, R.-H. *et al.* Stretchable, Transparent Graphene Interconnects for Arrays of Microscale Inorganic Light Emitting Diodes on Rubber Substrates. *Nano Letters* **11**, 3881–3886 (2011). URL https://pubs.acs.org/doi/10.1021/nl202000u.

[169] Zahab, A. & Firlej, L. Resistivity in C60 thin films of high crystallinity. *Solid State Communications* **87**, 893–897 (1993). URL https://linkinghub.elsevier.com/retrieve/pii/0038109893907242.

[170] Hamed, A., Sun, Y. Y., Tao, Y. K., Meng, R. L. & Hor, P. H. Effects of oxygen and illumination on the *in situ* conductivity of C 60 thin films. *Physical Review B* **47**, 10873–10880 (1993). URL https://link.aps.org/doi/10.1103/PhysRevB.47.10873.

[171] Arai, T. *et al.* Resistivity of single crystal C60 and effect of oxygen. *Solid State Communications* **84**, 827–829 (1992). URL https://linkinghub.elsevier.com/retrieve/pii/003810989290099U.

[172] Grillo, A. & Di Bartolomeo, A. A Current–Voltage Model for Double Schottky Barrier Devices. *Advanced Electronic Materials* **7**, 2000979 (2021). URL https://onlinelibrary.wiley.com/doi/10.1002/aelm.202000979.

[173] Nagano, T. *et al.* Output Properties of C 60 Field-Effect Transistors with Au Electrodes Modified by 1-Alkanethiols. *The Journal of Physical Chemistry C* **111**, 7211–7217 (2007). URL https://pubs.acs.org/doi/10.1021/jp0708751.

[174] Khurelbaatar, Z. *et al.* Temperature dependent current–voltage characteristics of Au/n-type Ge Schottky barrier diodes with graphene interlayer. *Journal of Alloys and Compounds* **650**, 658–663 (2015). URL https://linkinghub.elsevier.com/retrieve/pii/S0925838815307271.

[175] Li, H. *et al.* Temperature-dependent Schottky barrier in high-performance organic solar cells. *Scientific Reports* **7**, 40134 (2017). URL http://www.nature.com/articles/srep40134.

[176] Newville, M. *et al.* Lmfit: Non-Linear Least-Square Minimization and Curve-Fitting for Python. *Astrophysics Source Code Library* ascl:1606.014 (2016). URL https://ui.adsabs.harvard.edu/abs/2016ascl.soft06014N. ADS Bibcode: 2016ascl.soft06014N.

[177] Atalla, M. & Kahng, D. A new "Hot electron" triode structure with semiconductor-metal emitter. *IRE Transactions on Electron Devices* **9**, 507–508 (1962). URL http://ieeexplore.ieee.org/document/1473276/.

[178] Geppert, D. The metal-base transistor. *IRE Transactions on Electron Devices* **9**, 507–507 (1962). URL https://ieeexplore.ieee.org/document/1473277/.

[179] Crowell, C. & Sze, S. Hot-electron transport and electron tunneling in thin film structures **4** (1967).

[180] Gall, D. Electron mean free path in elemental metals. *Journal of Applied Physics* **119**, 085101 (2016). URL https://pubs.aip.org/jap/article/119/8/085101/143910/Electron-mean-free-path-in-elemental-metals.

[181] Rosencher, E., Glastre, G., Vincent, G., Vareille, G. & D'avitaya, F. A. Si/CoSi2/Si permeable base transistor obtained by silicon molecular beam epitaxy over a CoSi2 grating. *Electronics Letters* **13**, 699–700 (1986). URL https://www.infona.pl//resource/bwmeta1.element.ieee-art-000004256678.

[182] Bozler, C. & Alley, G. Fabrication and numerical simulation of the permeable base transistor. *IEEE Transactions on Electron Devices* **27**, 1128–1141 (1980). URL http://ieeexplore.ieee.org/document/1480789/.

[183] Bozler, C. O. Current prospects for the permeable base transistor. *Surface Science* **174**, 487–500 (1986). URL https://www.sciencedirect.com/science/article/pii/0039602886904589.

[184] Rosencher, E., Delage, S., Campidelli, Y. & Arnaud D'Avitaya, F. Transistor effect in monolithic Si/CoSi2/Si epitaxial structures. *Electronics Letters* **20**, 762 (1984). URL https://digital-library.theiet.org/content/journals/10.1049/el_19840519.

[185] Letourneau, P., Vincent, G., Perret, P., Badoz, P. & Rosencher, E. Si permeable-base transistor realization using a MOS-compatible technology. *IEEE Electron Device Letters* **10**, 550–552 (1989). URL http://ieeexplore.ieee.org/document/43136/.

[186] Yang, C.-Y. *et al.* Vertical organic triodes with a high current gain operated in saturation region. *Applied Physics Letters* **89**, 183511 (2006). URL https://pubs.aip.org/aip/apl/article/919221.

[187] Feng, C. *et al.* Copper phthalocyanine based hybrid p-type permeable-base transistor in vertical architecture. *Applied Physics Letters* **88**, 203501 (2006). URL https://pubs.aip.org/apl/article/88/20/203501/331894/Copper-phthalocyanine-based-hybrid-p-type.

[188] Kim, J. H., Yu, H., Liu, R., Kim, D. Y. & So, F. All Solution-Processed Inorganic/Organic Hybrid Permeable Metal-Base Transistor. *Small* **10**, 3650–3654 (2014). URL https://onlinelibrary.wiley.com/doi/10.1002/smll.201303959.

[189] Lüssem, B., Günther, A., Fischer, A., Kasemann, D. & Leo, K. Vertical organic transistors. *Journal of Physics: Condensed Matter* **27**, 443003 (2015). URL https://iopscience.iop.org/article/10.1088/0953-8984/27/44/443003.

[190] Xia, J., Chen, F., Li, J. & Tao, N. Measurement of the quantum capacitance of graphene. *Nature Nanotechnology* **4**, 505–509 (2009). URL https://www.nature.com/articles/nnano.2009.177.

[191] Hasegawa, T. & Takeya, J. Organic field-effect transistors using single crystals. *Science and Technology of Advanced Materials* **10**, 024314 (2009). URL http://www.tandfonline.com/doi/full/10.1088/1468-6996/10/2/024314.

[192] Gershenson, M. E., Podzorov, V. & Morpurgo, A. F. *Colloquium* : Electronic transport in single-crystal organic transistors. *Reviews of Modern Physics* **78**, 973–989 (2006). URL https://link.aps.org/doi/10.1103/RevModPhys.78.973.

[193] Menke, T., Ray, D., Meiss, J., Leo, K. & Riede, M. *In-situ* conductivity and Seebeck measurements of highly efficient n-dopants in fullerene C60. *Applied Physics Letters* **100**, 093304 (2012). URL https://pubs.aip.org/apl/article/100/9/093304/23756/In-situ-conductivity-and-Seebeck-measurements-of.

[194] Schubert, S. *et al.* Highly doped fullerene C60 thin films as transparent stand alone top electrode for organic solar cells. *Solar Energy Materials and Solar Cells* **118**, 165–170 (2013). URL https://linkinghub.elsevier.com/retrieve/pii/S0927024813004169.

[195] Song, Y., Zou, W., Lu, Q., Lin, L. & Liu, Z. Graphene Transfer: Paving the Road for Applications of Chemical Vapor Deposition Graphene. *Small* **17**, 2007600 (2021). URL https://onlinelibrary.wiley.com/doi/10.1002/smll.202007600.

[196] Pingel, P. & Neher, D. Comprehensive picture of p -type doping of P3HT with the molecular acceptor F 4 TCNQ. *Physical Review B* **87**, 115209 (2013). URL `https://link.aps.org/doi/10.1103/PhysRevB.87.115209`.

[197] Duong, D. T., Wang, C., Antono, E., Toney, M. F. & Salleo, A. The chemical and structural origin of efficient p-type doping in P3HT. *Organic Electronics* **14**, 1330–1336 (2013). URL `https://linkinghub.elsevier.com/retrieve/pii/S1566119913000840`.

[198] Nagamatsu, S. & Pandey, S. S. Ordered arrangement of F4TCNQ anions in three-dimensionally oriented P3HT thin films. *Scientific Reports* **10**, 20020 (2020). URL `https://www.nature.com/articles/s41598-020-77022-0`.

[199] Schilling, R. B. & Schachter, H. Neglecting Diffusion in Space-Charge-Limited Currents. *Journal of Applied Physics* **38**, 841–844 (1967). URL `https://pubs.aip.org/jap/article/38/2/841/288060/Neglecting-Diffusion-in-Space-Charge-Limited`.

Acronyms

AFM Atomic Force Microscopy. 2, 11, 18, 19, 23, 25–28, 55, 57, 58, 72, 73, 85, 98, 99, 127, 138, 148

APS Automated Probe Station. 14, 16, 18

CAFM Conductive Atomic Force Microscopy. 98, 99

CPD Contact Potential Difference. 55, 144

CVD Chemical Vapour Deposition. 7, 10–15, 23, 24, 26–29, 32, 35, 36, 41, 43, 54, 57, 58, 70, 71, 73, 83, 84, 88, 96, 98–100, 123, 125, 128–131

DIW de-ionized water. 12, 13, 36, 123–126

DMSO Dimethyl sulfoxide. 124, 125

DNTT Dinaphtho[2,3-b:2,3-f]thieno[3,2-b]thiophene. 9

DOS Density of States. 25

DSB Double Schottky Barrier. 71, 74, 76–81, 83, 86, 99, 155, 156, 158

DUT Device Under Test. 17, 18

EBPVD e-beam physical vapour deposition. 17, 54, 84, 124

F4TCNQ 2,3,5,6-Tetrafluoro-7,7,8,8-tetracyanoquinodimethane. 68, 100

F6TCNNQ 1,3,4,5,7,8-hexafluorotetracyanonaphthoquinodimethane. 68

FET Field Effect Transistor. 18, 26, 29, 68, 94

FETs Field Effect Transistors. 5

FIB Focused Ion Beam. 57, 85

FN Fowler-Nordheim. 71, 75, 78–81, 83, 86, 159

GFET Graphene Field Effect Transistor. 7, 14, 16, 23–25, 27, 35, 40, 42, 43, 46, 49, 93

GFETs Graphene Field Effect Transistors. 14, 18, 23–26, 28–36, 38, 40–44, 46, 48, 92, 98–100, 127, 130–135, 137

Gr Graphene. 1, 3, 5–7, 9–11, 15, 16, 19, 23–27, 33, 35, 42, 52, 53, 55, 57–59, 61, 62, 65, 66, 68, 70–74, 76, 77, 79–81, 83, 84, 87, 89, 90, 92, 93, 95, 98–100, 124, 125, 128, 129, 138, 143, 144, 146–148, 155, 156

HMDS Hexamethyldisilazan. 125

HOMO highest occupied molecular orbital. 24, 25, 33, 67, 68, 81, 164

IoT Internet of Things. 40

IPA Isopropyl alcohol. 123–125

IPES Inverted Photoelectron Spectroscopy. 25

KPFM Kelvin Probe Force Microscopy. 53, 55, 66, 99, 144

LUMO lowest unoccupied molecular orbital. 24, 25, 33, 67, 81, 83

MTE Modified TE. 60, 61, 75, 77

OLED organic light emitting diode. 53, 71

OLEDs Organic Light Emitting Diodes. 97

OSC Organic Semiconductor. 1, 3, 5–7, 9–11, 16, 19, 23, 25, 52, 53, 59–62, 68, 71, 75, 76, 80, 82, 83, 87, 89, 90, 92–96, 98–101, 132, 157, 161, 165

OSCs Organic Semiconductors. 1, 7, 9, 10, 25, 33, 87–89, 92–94, 99

OTFT Organic Thin Film Transistor. 7, 9, 88

OTFTs Organic Thin Film Transistors. 8, 87

P3HT poly(3-hexylthiophene-2,5-diyl). 7, 14–16, 19, 52–55, 57–62, 64–68, 71, 98–100, 124, 125, 138, 139, 141, 143, 144, 146, 147

PBT Permeable-Base Transistor. 88

PFE Poole-Frenkel Emission. 60

PMMA Poly(methyl methacrylate). 12, 15, 16, 30, 36, 52, 53, 123–126

RF Radio-Frequency. 9, 71

RIE Reactive ion etching. 12, 14–17, 36, 49, 54, 84, 96, 99, 101, 123, 126

RR regio-regular. 14, 54

SCL Space-Charge-Limited. 56, 61, 63, 65–68, 142, 145

SEM Scanning Electron Micrscopy. 57, 58, 72, 73, 85, 138, 148, 162

TE termionic emission. 53, 56, 60–62, 65–68, 75, 79–81, 83, 99, 142, 147

TLM Transfer Length Method. 23, 32, 33, 38, 134

UPS Ultraviolet Photoelectron Spectroscopy. 25

UV Ultraviolet. 125

vdW van der Waals. 1, 5, 23, 52, 53, 71, 73, 80

VOFET Vertical Organic Field Effect Transistor. 7, 9

VOFETs Vertical Organic Field Effect Transistors. 3

VOGBT Vertical Organic Graphene Base Transisor. 2, 3, 10, 87, 89–92, 95–97, 100, 101

VOGBTs Vertical Organic Graphene Base Transisor. 97

VOPBLET Vertical Organic Permable Base Light Emitting Transistor. 97

VOPBT Vertical Organic Permeable Base Transisor. 8–10, 87–91, 95, 97, 98, 100

VOPBTs Vertical Organic Permeable Base Transistors. 8, 97

VOTs Vertical Organic Transistors. 1, 5

Appendices

A Fabrication recipes

Chemical vapour deposition of graphene on Cu foils

(i) *Pre-cleaning of the Cu foils*
The foils are ultrasonicated in Acetone, rinsed with Isopropyl alcohol (IPA) and dried with N_2. Then, the foils are placed in Acetic Acid (CH_3COOH) for 30 min, rinsed in de-ionized water (DIW) and Ethanol, and dried with N_2.

(ii) *CVD growth of graphene on Cu foils*
The copper foils are pre-annealed at 1000 °C for 1 h in a H_2 (20 sccm) and Ar (200 sccm) atmosphere in the CVD oven (ca. 1 mbar). Then, graphene grows for 35 min in a CH_4 (0.05 sccm), H_2 (20 sccm) and Ar (200 sccm) atmosphere under a pressure of ca. 120 mbar. After the CH_4 flow is stopped, the CVD oven is left to cool down to room temperature (at ca. 1 mbar).

(iii) *Deposition of the protective PMMA layer on graphene*
The graphene grown on the front side of the Cu foil is protected with a PMMA layer. The PMMA is spin coated on the topside of the Cu foils with graphene at 1000 rpm for 1 min.

(iv) *RIE removal of the Gr backside*
The graphene grown on the backside of the Cu foil is removed by Reactive ion etching (RIE). The foils is placed in the RIE chamber with the PMMA layer facing downwards. Then, the unprotected graphene is exposed to RIE plasma for 2 min and a gas flow of O_2 and Ar was set to 15 sccm and 30 sccm, respectively.

Transfer of large area graphene from Cu foils to devices

(i) *Copper foils edges cutting*
Roughly, a 1 mm wide strip was cut from each side of the Cu foils to remove the excess of PMMA built up during the spin-coating and ensure uniform etching of the Cu foils.

(ii) *Ferric chloride $FeCl_3$ etching of Cu foil*
The Cu substrate was etched away in a Ferric Chloride ($FeCl_3$, Transene CE-

100) bath for 1 h, until the Cu foil was complety dissolved and only the PMMA layer floating of the etchant was still visible.

(iii) *Transfer of the graphene foils to DIW*
The etchant is slowly replaced with DIW, until the solution appears clear and transparent. Then, the foils are transferred in larger glasses filled with DIW, further diluting the possible residual etchant.

(iv) *HCl cleaning of FeCl*
Using the same procedure, the remaining Gr/PMMA sheet was placed in Hydrochloric acid (HCl 10%) for 5 min.

(v) *Transfer in DIW*
The HCl is slowly replaced with DIW before transferring the foils in larger glass filled with DIW to furhter dilute the possible residual HCl.

(vi) *Transfer onto target substrate*
Graphene can be transferred on the target substrate. The substrate is dipped into the DIW at an angle of approximately 45° to gently capture the floating graphene.

(vii) *Drying in air and vacuum*
After the transfer, the substrate is left to dry in air for approximately 1h. Then, the sample is dried overnight in a vacuum oven (ca. 1 mbar, 80 °C).

(viii) *Removal of PMMA*
The sample (substrate/Gr/PMMA) is placed first in Acetone for 1 h (at 55 °C), then in IPA (at 55 °C), before finally being dried with N_2. The sample is ready for the next fabrications step.

Vertical metal-organic-graphene stacks

Figure 7 shows the main fabrication steps of the Au / P3HT / Gr heterostructure, which consists in

(a) *Patterning of the bottom electrodes*
Ti (5 nm) / Au (30 nm) electrodes are fabricated on a 4 inches Si (525 µm) / SiO_2 (300 nm) wafer, which is pre-cleaned in oxygen plasma (600 W for 5 min). The electrodes (Ti / Au) are deposited by e-beam physical vapour deposition (EBPVD) and patterned by lift-off in DMSO at 100 °C for 30 min. The resist for the lift-off (AZ2020nlof) is spin-coated (4000 rpm for 60 s), exposed to

UV light (lamp intensity $11\,\mathrm{mW/cm^2}$) through an optical mask, and then developed (AZ726mif, 35 s).

(b) *Preparation of the lift-off resist*

The chip with pre-patterned electrodes (Si / SiO$_2$ / Ti / Au) is ultra-sonicated in Acetone for 5 min, rinsed with IPA and blown dry with nitrogen. Then, it is exposed to oxygen plasma at 600 W for 5 min. After HMDS treatment, the chip is coated with a double layer positive optical resist: first, the chip is spin-coated with a LOR5B resist (4000 rpm, 40 s) and backed at 180 °C for 5 min. Then, it is spin-coated with an AZ1505 positive resist (4000 rpm, 40 s) and backed at 110 °C for 1 min. The device area is exposed for 1.8 s s to UV light (lamp intensity $11\,\mathrm{mW/cm^2}$, dose 20 mJ) through an optical mask. Finally, the exposed resist is developed in AZ400K (400K:DIW, 1:4) for 25 s and rinsed with DIW.

(c) *P3HT deposition and patterning*

A 100 nm film of P3HT is obtained by spin-coating $10\,\mathrm{mg\,mL^{-1}}$ solution of P3HT in chlorobenzene (1000 rpm for 60 s)) on the substrate. Subsequently, the P3HT film is patterned by lift-off in DMSO (5 min). The chip is then rinsed in de-ionized water, blown dry with nitrogen and finally annealed overnight at 100 °C in vacuum ($\approx 1\,\mathrm{mbar}$).

(d) *CVD graphene transfer*

CVD graphene foil (Cu / Gr / PMMA) is placed to float in a copper etchant (Transene CE-100) for 1 h, the PMMA layer facing upwards. Once the copper is completely etched (Gr / PMMA), the etchant is removed and replaced with DIW, twice. Then, the foil is transferred to a 10% HCL cleaning solution for 5 min and transferred back to DIW, twice. The floating graphene foil (Gr / PMMA) is transferred onto the substrate (Si / SiO$_2$ / Au / P3HT / Gr / PMMA) and let dry in air for 1 h.

(e) *PMMA removal from graphene*

The chip is annealed overnight at 80 °C in vacuum ($\approx 1\,\mathrm{mbar}$). The top PMMA layer is removed in Acetone (5 min) and the chip annealed again overnight at 80 °C in vacuum ($\approx 1\,\mathrm{mbar}$).

(f) *RIE patterning of the graphene top electrode*

The chip is first spin-coated with a 50 K PMMA resist (AR-P 632.06, 4000 rpm for 60 s), then with an AZ1505 optical resist (4000 rpm for 40 s) and backed at 110 °C for 1 min. The device area is exposed for 1.8 s to UV light (lamp

intensity 11 mW/cm2) through an optical mask. The exposed optical resist is developed in AZ400K (400K:DIW, 1:4) for 15 s and rinsed with DIW. Then, RIE is used to remove the first layer of PMMA 50 K and graphene (O_2, 30 sccm, 25 W).

(g) *PMMA / Optical resist removal from graphene*
The PMMA / Optical resist protecting the graphene electrode is removed with Acetone (1 min), then the chip is rinsed in DIW and blown dry with nitrogen.

B   Graphene field effect transistors

Atomic Force Microscopy (AFM)

a) Chip 1: C60-GFETs

b) Chip 1: C60 on SiO$_2$

c) Chip 2: Pentacene-GFETs

d) Chip 2: Pentacene on SiO$_2$
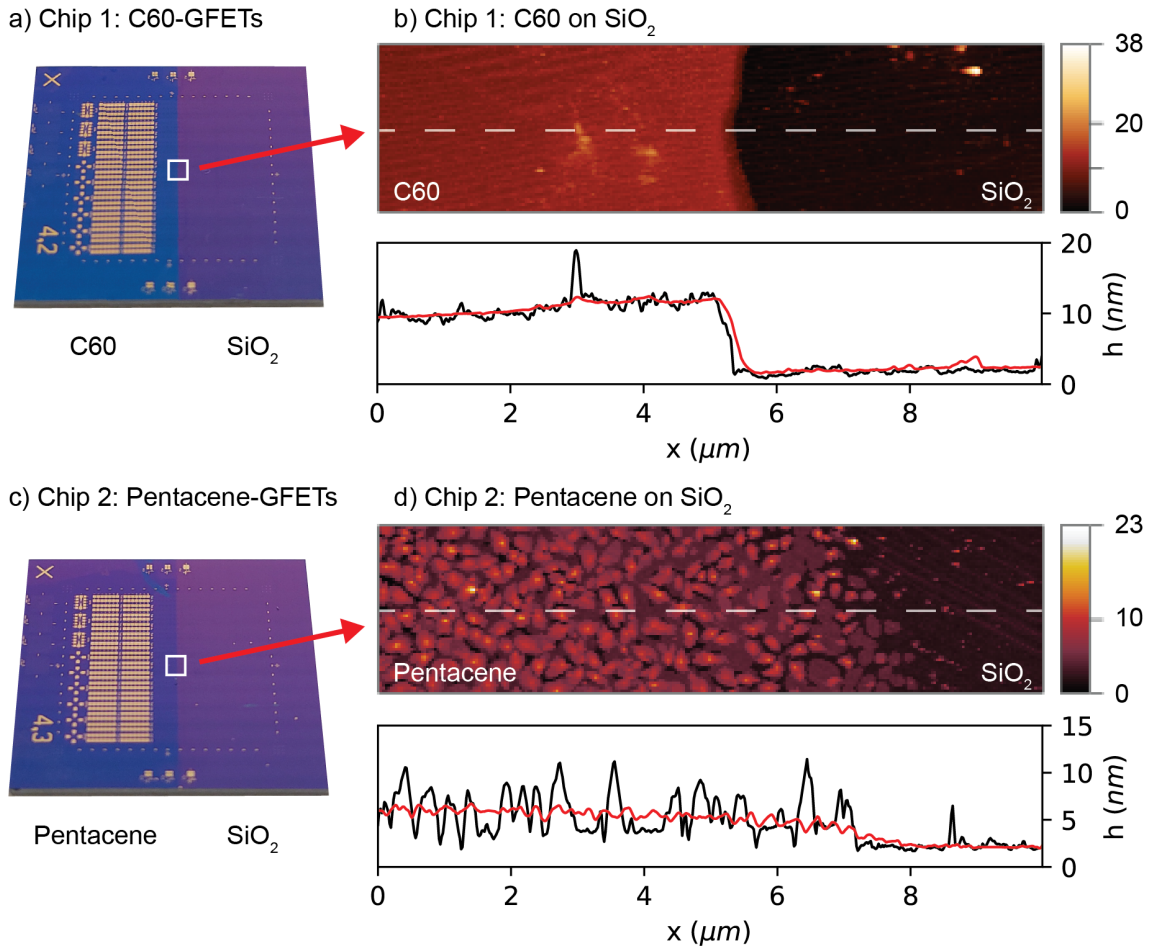
Figure 32: (a) Photograph of Chip 1 including the C60-GFETs. The white square show the region where the thickness of the C60 film was measured. (b) AFM height image and profile taken on Chip 1 with the set of C60-GFETs. The right part, which was covered during the thermal evaporation of C60, shows the bare SiO$_2$ substrate. The AFM profile shows that the C60 film on SiO$_2$ is uniform and the measured average thickness is ca. 10 nm. The black line is the AFM profile taken along the white dashed line on the AFM image. The red line is the mean profile value of the whole image. (c) Photograph of Chip 2 including the Pentacene-GFETs. (d) AFM height image and profile taken on the chip with the set of Pentacene-GFETs. The right part, which was covered during the thermal evaporation of Pentacene, shows the bare SiO$_2$ substrate. The Pentacene film is covering large part of the substrate and shows the typical thin film phase structure of Pentacene with an average thickness of ca. 5 nm. The red line is the mean profile value of the whole image
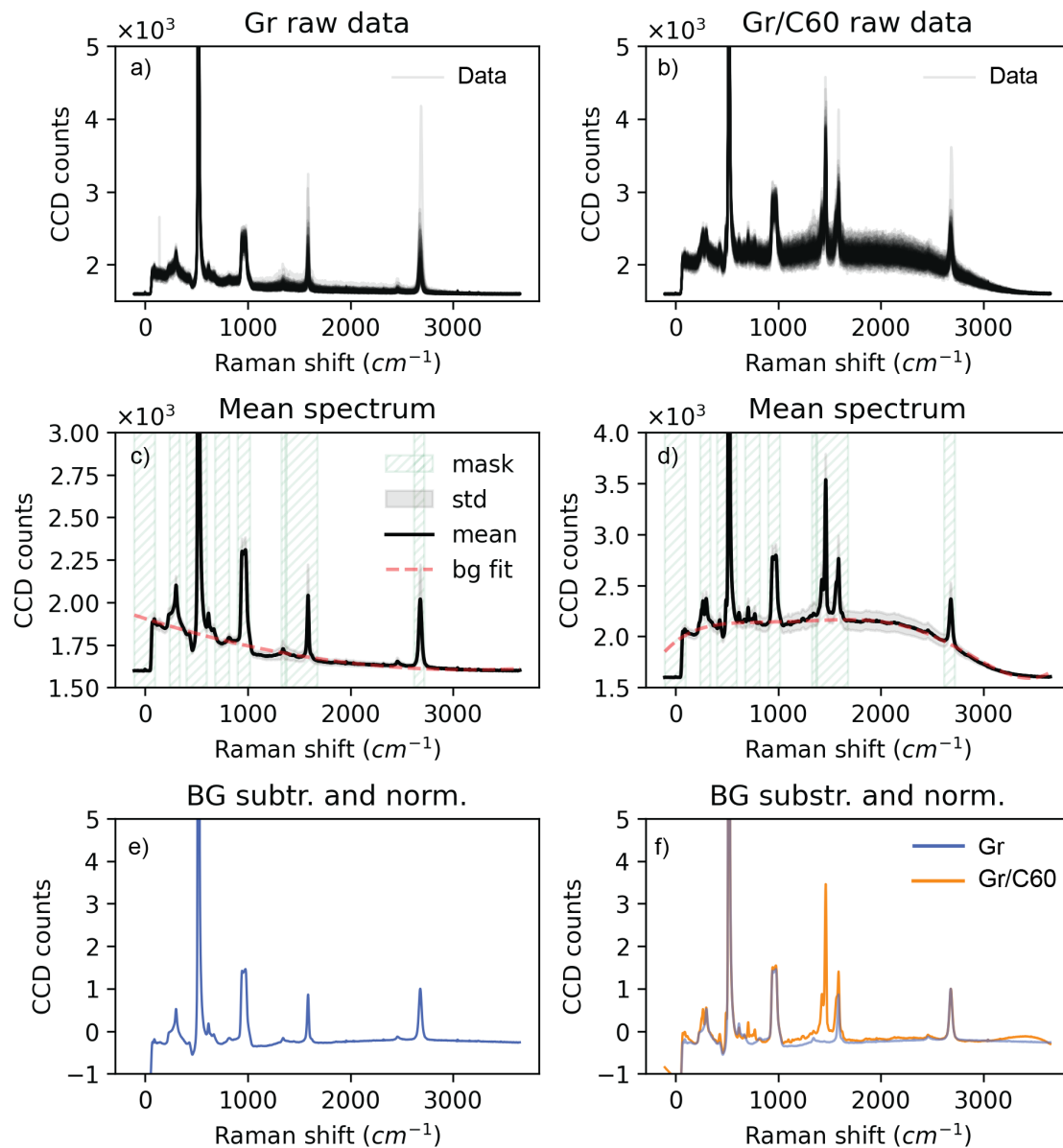
Raman spectroscopy

Figure 33: Raman spectrum of the Gr/C60 hybrid heterostructures. (a) Raman spectra of the 150 pristine CVD Gr channels. (b) Raman spectra of the 150 Gr/C60 channels. (c) Average Raman spectrum of the 150 measurements of the pristine CVD Gr in (a). The red dashed line is the polynomial fit (degree 2) of the background. The green hatched areas (mask) are not considered in the polynomial fit. (d) Average Raman spectrum of the 150 measurements of the Gr/C60 heterostructures in (b). The red dashed line is the polynomial fit (degree 5) of the background. The green hatched areas (mask) are not considered in the polynomial fit. (e) Pristine CVD graphene Raman spectrum after background removal and normalization to the 2D peak of graphene. (f) Raman spectrum of the Gr/C60 heterostructure after background removal and normalization to the 2D peak of graphene.
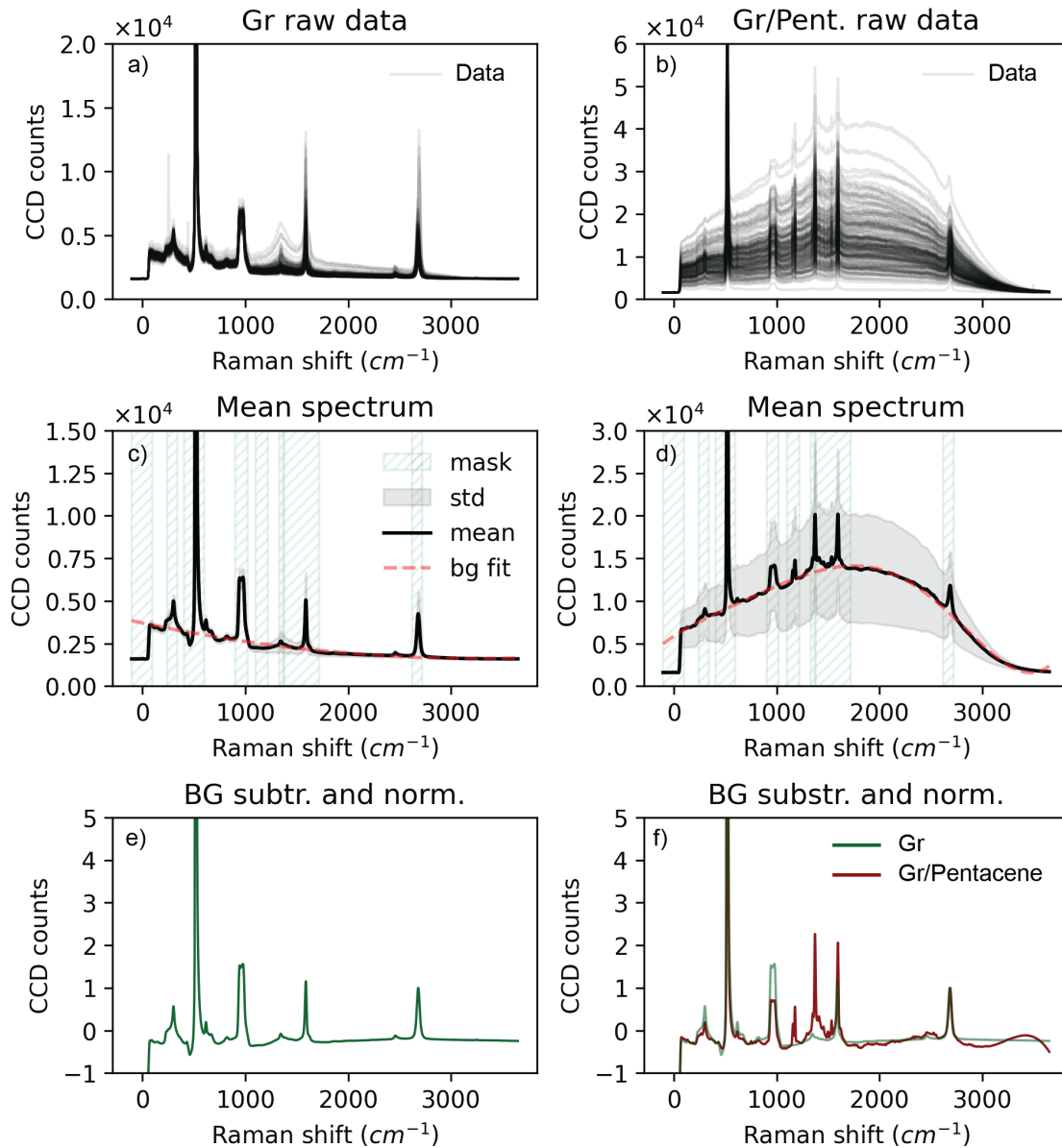
Figure 34: Raman spectrum of the Gr/Pentacene heterostructures. (a) Raman spectra of the 150 pristine CVD Gr channels. (b) Raman spectra of the 150 Gr/Pentacene channels. (c) Average Raman spectrum of the 150 measurements of the pristine CVD Gr in (a). The red dashed line is the polynomial fit (degree 2) of the background. The green hatched areas (mask) are not considered in the polynomial fit. (d) Average Raman spectrum of the 150 measurements of the Gr/Pentacene heterostructure in (b). The red dashed line is the polynomial fit (degree 5) of the background. The green hatched areas (mask) are not considered in the polynomial fit. (e) Pristine CVD graphene Raman spectrum after background removal and normalization to the 2D peak of graphene. (f) Raman spectrum of the Gr/Pentacene heterostructure after background removal and normalization to the 2D peak of graphene.
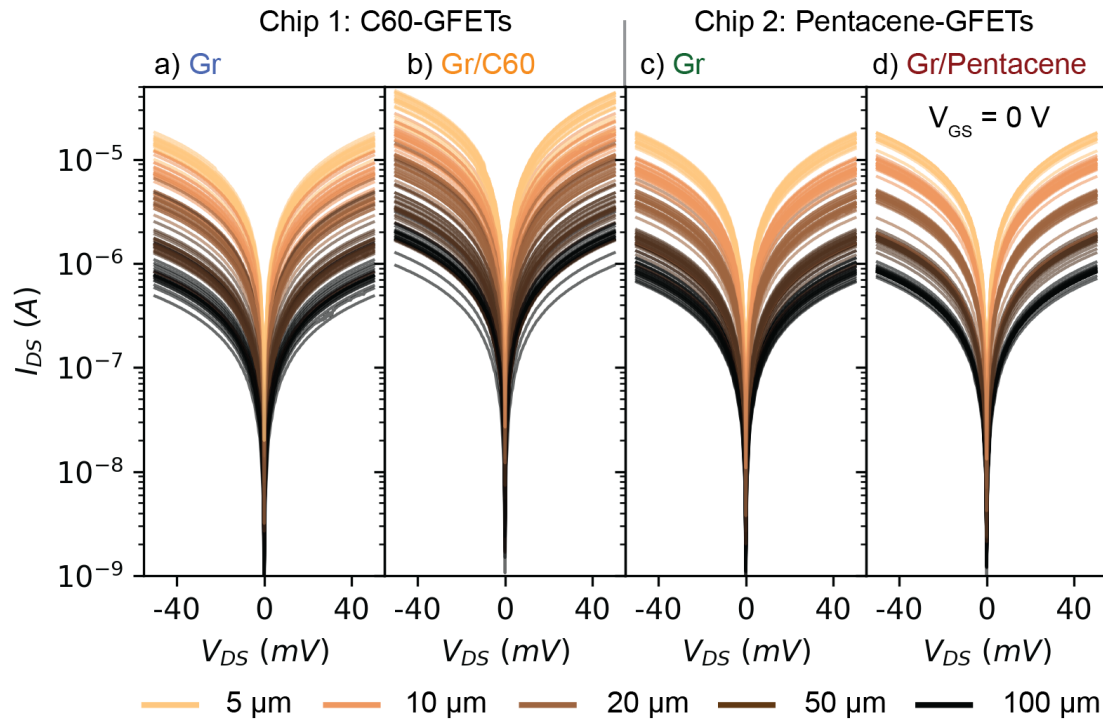
Electrical characterization

Figure 35: Output characteristic (I_{DS} vs. V_{DS}) of the GFETs measured at zero gate-to-source voltage ($V_{GS} = 0V$). (a) Output characteristics of pristine CVD graphene FETs before C60 deposition (Chip 1, 101 devices, all L included). (b) Output characteristics of the C60-GFETs (Chip 1, 101 devices, all L included). (c) Out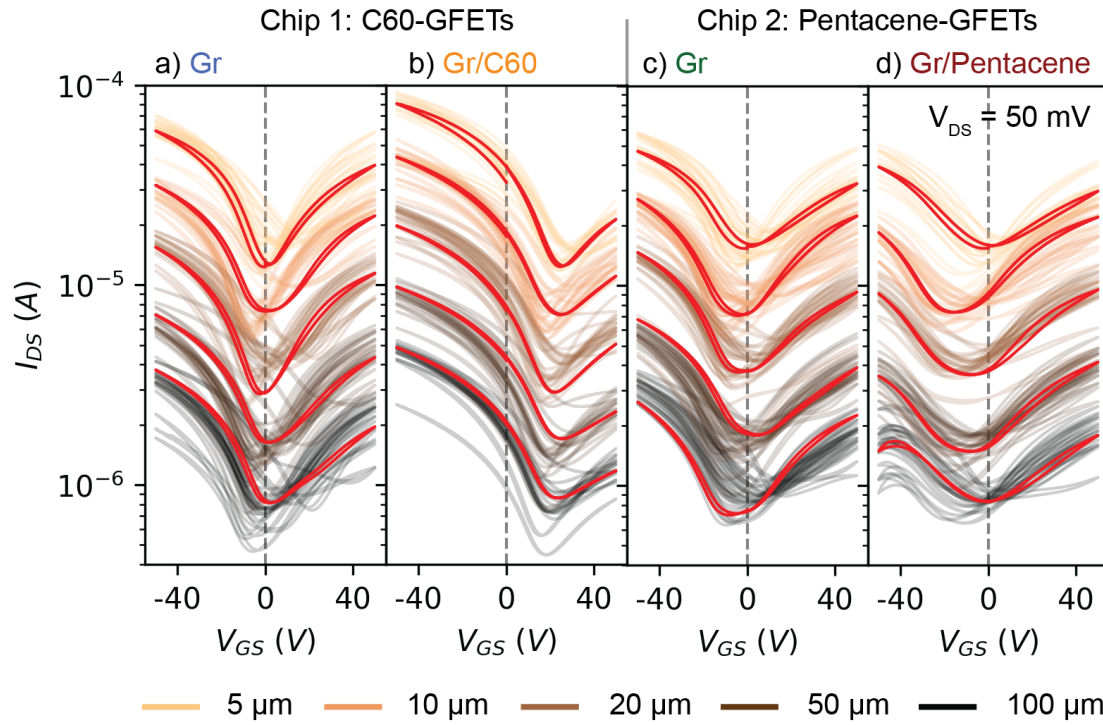put characteristics of pristine CVD graphene before Pentacene deposition (Chip 2, 119 devices, all L included). (d) Output characteristics of the Pentacene-GFETs (Chip 2, 98 devices, all L included).

Figure 36: Transfer characteristics (I_{DS} vs. V_{GS}) of the GFETs, the drain-to-source voltage is kept constant at $VDS = 50\,\mathrm{mV}$ for all measurements. The graphs show a representative forward/backward sweep for each channel length highlighted in red. The backward and forward sweep are virtually identically and only the backward continuous sweep is considered in this work. (a) Transfer characteristics of pristine CVD graphene FETs before C60 deposition (Chip 1, 101 devices, all L included). (b) Transfer characteristics of the C60-GFETs (Chip 1, 101 devices, all L included). (c) Transfer characteristics of pristine CVD graphene before Pentacene deposition (Chip 2, 119 devices, all L included). (d) Transfer characteristics of the Pentacene-GFETs (Chip 2, 98 devices, all L included).
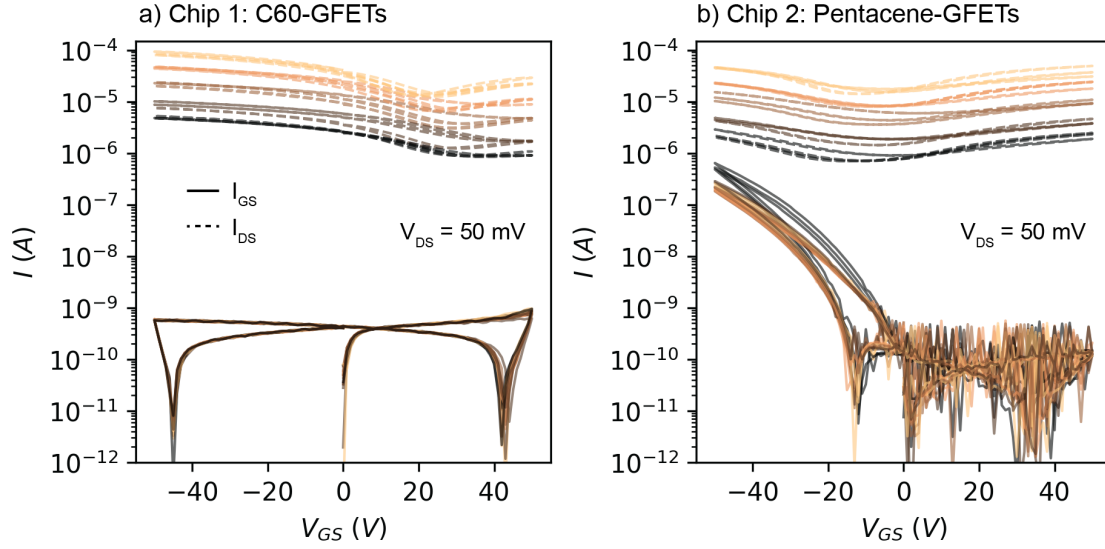
Figure 37: GFETs I_{GS} (gate-to-source current) vs. I_{DS} of 3 representative devices per channel length L. (a) C60-GFETs. $I_{GS} \ll I_{DS}$ for the whole gate-to-source voltage range ($-50\,\text{V}$ to $50\,\text{V}$). (b) Pentacene-GFETs. $I_{GS} \ll I_{DS}$ for positive V_{GS}. The I_{GS} increases for negative gate voltages and the ratio $I_{DS}/I_{GS} \simeq 10$ for $V_{GS} < -40\,\text{V}$ for the longer graphene channels ($L = 100\,\mu\text{m}$). $I_{DS}/I_{GS} > 100$ for the shorter channels in the whole V_{GS} range ($-50\,\text{V}$ to $50\,\text{V}$). The increasing I_{GS} for negative V_{GS} in Pentacene-GFETs is possibly ascribed to the gating of the full film of Pentacene (p-type OSC), which becomes more conductive at negative gate voltages. Since I_{GS} is not limited, the transfer characteristics of the GFETs and the conclusions of this work are not affected.
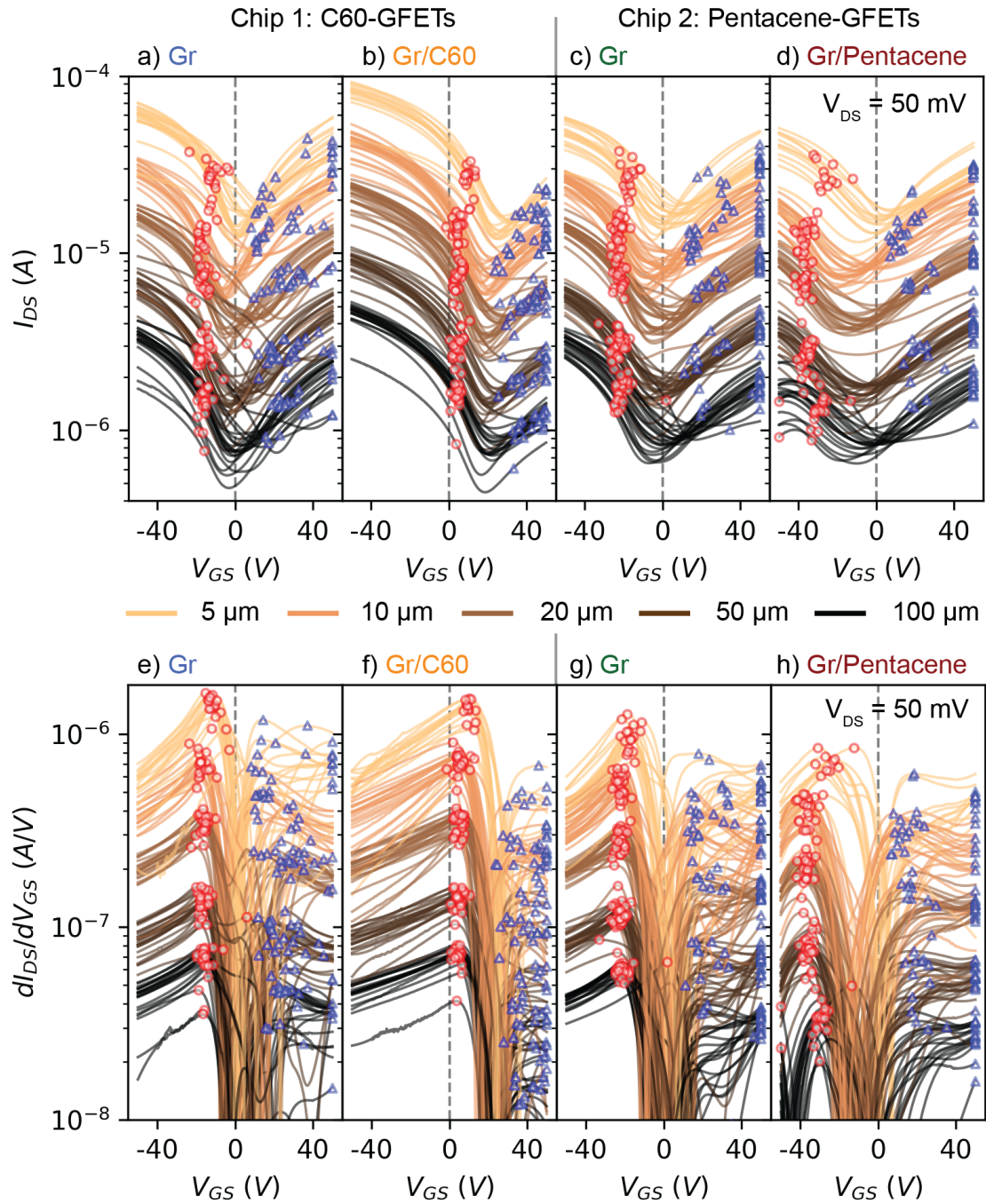
Figure 38: (a)-(d) Transfer characteristics (I_{DS} vs. V_{GS}) of the GFETs before and after the deposition of the C60 and Pentacene molecules. (e)-(h) Numerical derivative of the transfer characteristics (dI_{DS}/dV_{GS} vs. V_{GS}) of the GFETs before and after the deposition of the C60 and Pentacene molecules. The red circles show the maximum of the derivative for $V_{GS} < V_{GS}^{Dirac}$ that is used to calculate the field effect hole mobility using Eq. 3. The blue triangles show the maximum of the derivative for $V_{GS} > V_{GS}^{Dirac}$ that is used to calculate the field effect electron mobility using Eq. 3.
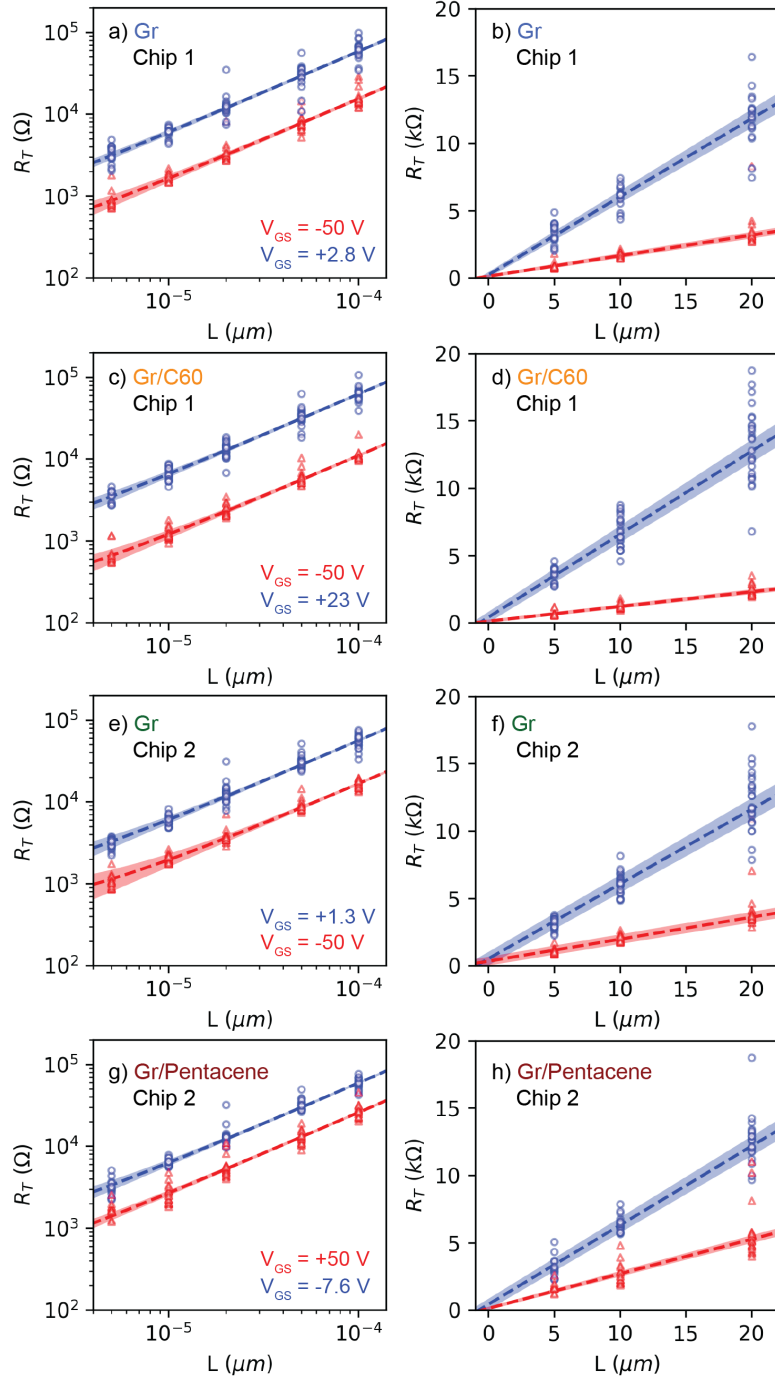
Figure 39: Total resistance (R_T) vs. channel length (L) of the GFETs. The sheet resistance (R_S) and contact resistance (R_C) are obtained from the slope and intercept of the linear regression of the data in the Transfer Length Method (TLM).The red and blue dashed lines are the results of the linear regressions for gate voltages of $\pm 50\,\mathrm{V}$ and V_{GS}^{Dirac}, respectively. Figure 14 shows the results of the linear regression for all the gate voltages in the range $-50\,\mathrm{V}$ to $50\,\mathrm{V}$. (a)-(b) R_T vs. L of the GFETs before deposition of C60. (c)-(d) R_T vs. L of the GFETs after deposition of C60.(e)-(f) R_T vs. L of the GFETs before deposition of Pentacene. (g)-(h) R_T vs. L of the GFETs after deposition of Pentacene.

Length (μm)	C60-GFETs		Pentacene-GFETs	
	Gr	Gr/C60	Gr	Gr/Pentacene
5	19	15	18	13
10	16	21	27	21
20	21	25	26	22
50	24	22	26	24
100	21	18	22	18
Working	101	101	119	98
Total	150	150	150	150

Table 3: GFETs measurements population overview. The table shows the number of electrical measurements considered in the analysis. The working device that were considered all show a linear output characteristic (I_{DS} vs. V_{DS}) in the range $\pm 50\,\text{mV}$ and the typical graphene field effect transistor transfer characteristic (I_{DS} vs. V_{GS}) in the range $\pm 50\,\text{V}$ at a constant $V_{DS} = 50\,\text{mV}$.

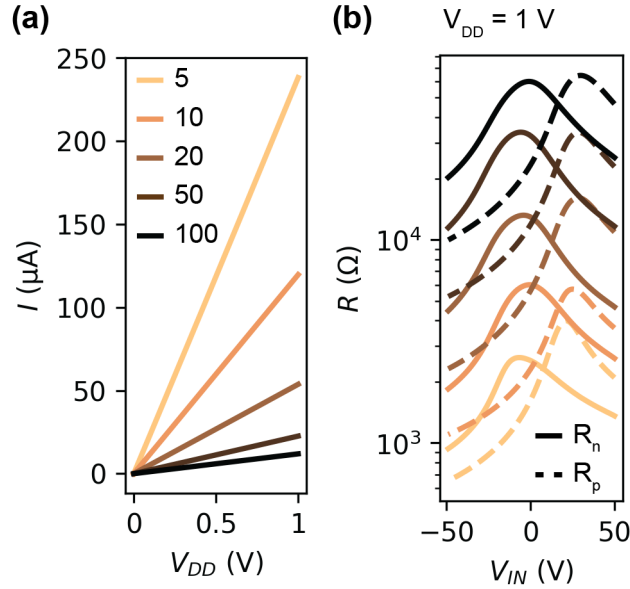# C   Complementary Inverters

Electrical characterization

Figure 40: (a) I vs. V_{DD} for channel length L = 5, 10, 20 and 50 μm. (b) R_n (solid line) and R_p (dashed line) vs V_{IN} of the inverter for channel length L = 5, 10, 20 and 50 μm, at $V_{DD} = 1V$.

Fig. 40 shows (a) output characteristic (I vs V_{DD}) and (b) transfer resistances (R vs V_{IN}) of the graphene complementary inverters. For the circuit simulations, the resistances $R_{n,p}(V_{IN})$ were extrapolated by fitting a polynomial in the range 0 - 20 V.

L (μm)	V_{swing} (V)	A (10^{-2})	P (μW)	f_c (GHz)
5 ± 0.2	0.29 ± 0.04	1.77 ± 0.10	240 ± 9.8	27.9 ± 1.47
10 ± 0.2	0.28 ± 0.03	1.79 ± 0.08	120 ± 3.9	8.29 ± 0.18
20 ± 0.2	0.33 ± 0.03	2.01 ± 0.08	54 ± 1.4	1.77 ± 0.02
50 ± 0.2	0.32 ± 0.03	1.95 ± 0.08	25 ± 0.6	0.32 ± 0.00
100 ± 0.2	0.28 ± 0.03	1.78 ± 0.07	12 ± 0.3	0.08 ± 0.00

Table 4: Parameters of the graphene complementary measured at fixed $V_{DD} = 1\,$V and digital input signal within $0\,$V to $20\,$V. The voltage swing is given by $V_{swing} = V_{OH} - V_{OL}$. The cut-off frequency of the inverters is calculated as $f_c = 1/4\pi R_{n//p}C_{ox}$.

Table 4 provides the main parameters of the graphene inverters that were fabricated and measured in this study. The parameters were extrapolated at fixed $V_{DD} = 1\,$V

and for a digital input signal within $0\,\mathrm{V}$ to $20\,\mathrm{V}$. The voltage swing is given by $V_{swing} = V_{OH} - V_{OL}$, while the static power dissipation is calculated at $V_{in} = 0V$ and the cut-off frequency of the inverters is calculated as $f_c = 1/4\pi R_{n//p}C_{ox}$. Assuming that the channel dimensions uncertainty (ΔL and ΔW) is approximately $0.2\,\mathrm{\mu m}$ and that the graphene sheet resistance is about $R_{S,n} \approx 3\,\mathrm{k\Omega}$, the uncertainty of V_{swing} is calculated as follows:

$$\Delta V_{swing} \approx R_{S,n}I_{DD}\sqrt{\left(\frac{\Delta L}{W}\right)^2 + \left(\frac{L\Delta W}{W^2}\right)^2} \tag{18}$$

while the power uncertainty is approximately $\Delta P = \Delta V_{swing}I_{DD}$, and the frequency f_c uncertainty is is given by:

$$\Delta f_c \approx \frac{t}{\pi R_{S,n}\epsilon_0\epsilon_r}\sqrt{\left(\frac{\Delta L}{L^3}\right)^2} \tag{19}$$

Similarly, the error on the voltage gain A is extrapolated from the expression:

$$\Delta A \approx A\sqrt{\left(\frac{\Delta L}{L}\right)^2 + \left(\frac{\Delta W}{W}\right)^2} \tag{20}$$

However, the variability between graphene-based inverters possibly depends on other factors, including the sheet and contact resistance of graphene. For detailed statistics on the variability between GFETs, refer to Chapter 4.
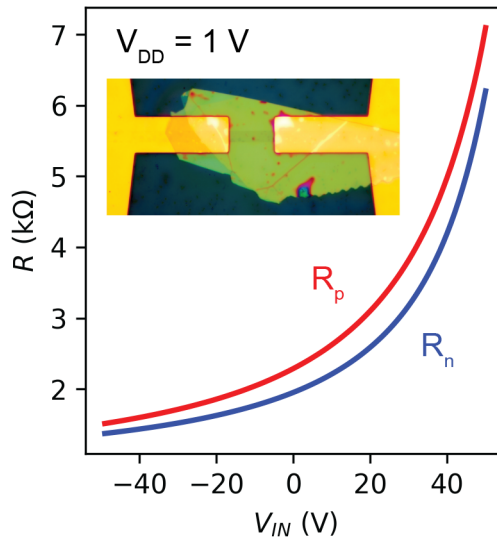

Figure 41: Resistance R vs. input voltage V_{IN} measured on a representative complementary inverter after hBN encapsulation of the two GFETs. The inset shows an optical microscope image of an encapuslated GFET, the channel length is $L = 20$ μm. The transfer resistances show that the inverter characteristic is lost after encapsulation.

D   Charge transport across Au-P3HT-Gr
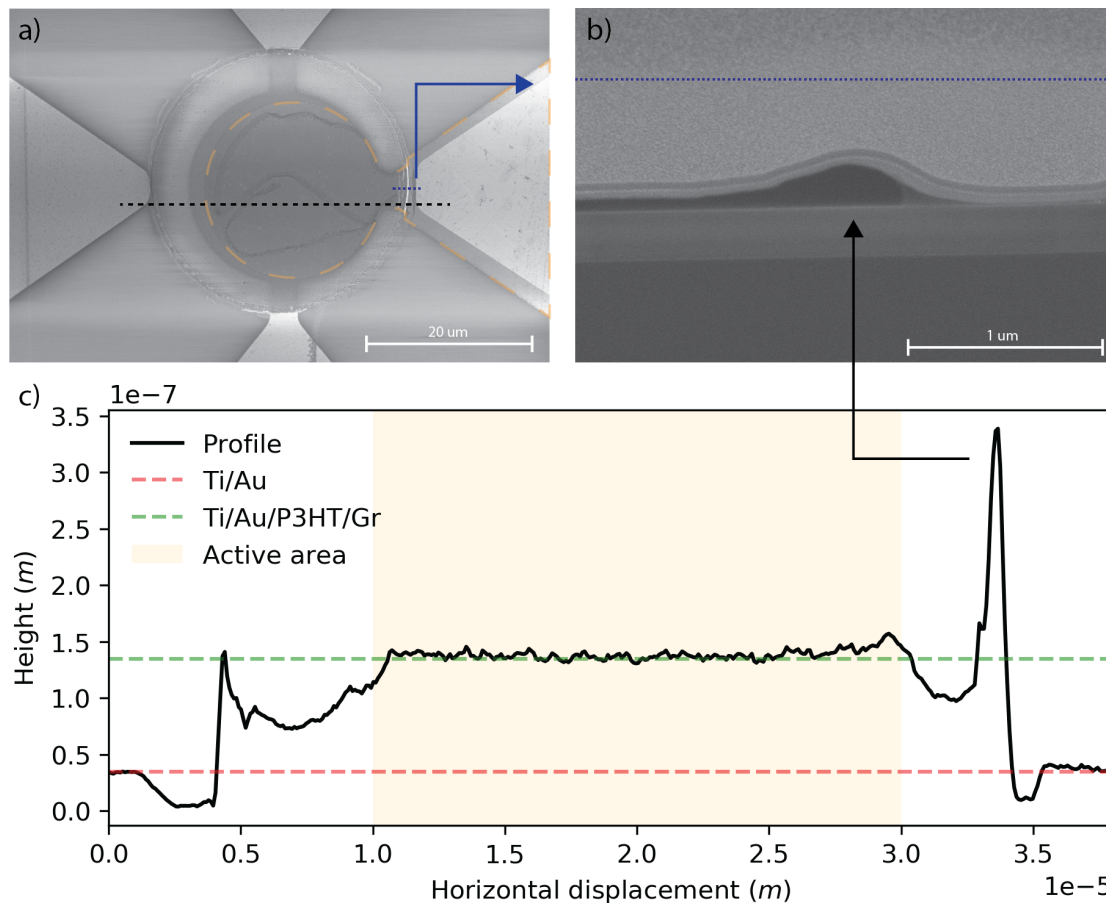
FIB/SEM/AFM characterization

Figure 42: SEM images. (a) Top view of a representative device. The orange dashed line shows the contour of the graphene electrode. The blue dashed line shows the location of the cross-section of (b). (b) Cross-section showing the right edge of P3HT. (c) AFM height profile of the Au / P3HT / Gr stack. The red dashed line show the height of the Ti / Au electrodes, i.e. 35 nm. The green dashed line represent the height of the Ti / Au / P3HT / Gr stack, i.e. 135 nm. From this, the deduced thickness of the P3HT layer is roughly 100 nm.

Figure 42a shows the SEM image and of a representative device. The graphene electrode is clearly visible and contoured with an orange dashed line. Graphene bilayers are distinguishable on the Au side contact. Figure 42b and 42c shows the cross-section corresponding to the dotted blue and dashed black line, respectively, in Figure 42a. The thickness of the P3HT film in the device center is uniform, while it is not on the device edge, where a higher ring possibly due to capillary/adhesion forces of the P3HT to resist prior to lift-off is observed. Although not desirable, the

high edge does not affect the geometry of the device, which is entirely dictated by the region where the bottom and the top electrodes superimpose (active area shown in Figure 42c), and does represent an issue for the graphene electrode since it can easily adapt to the smooth shape of the P3HT edge (Figure 42b).
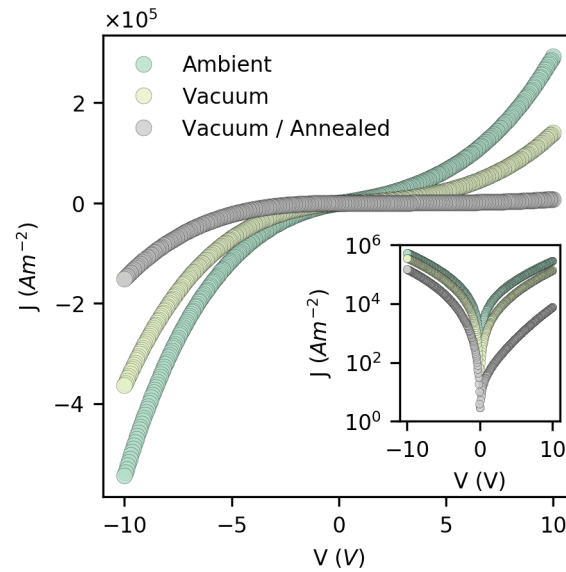
Electrical characterization

Figure 43: J-V traces of a 10 µm wide vertical Au / P3HT / Graphene device in ambient, in vacuum and in vacuum after annealing at 110 °C for 12 h. The inset shows the same traces on log scale.
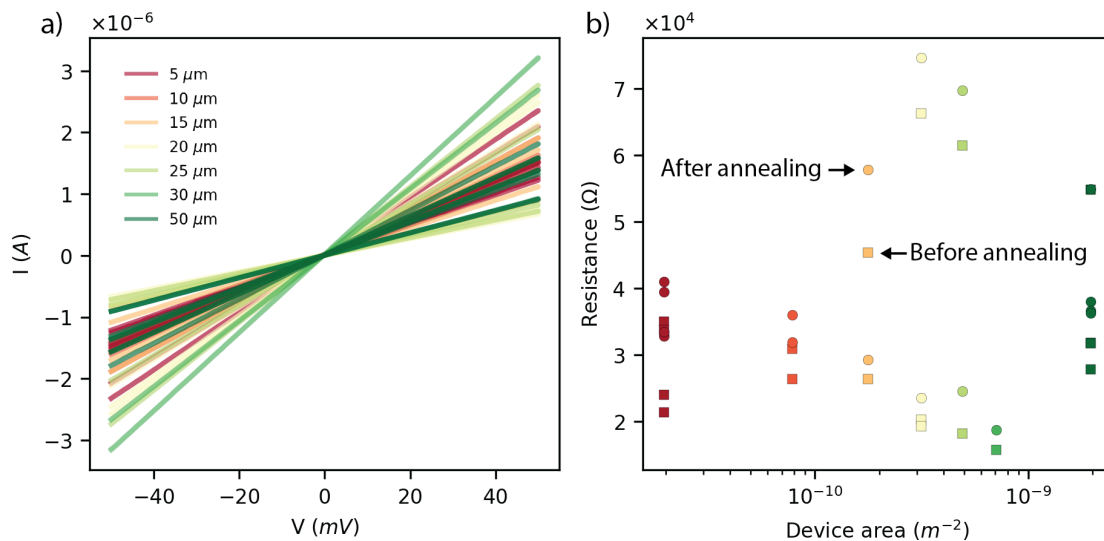
Figure 44: Graphene in-plane conductivity measurements. The total number of samples shown in the plot is 17. (a) Measured current vs. bias in the devices. Square symbols represent the devices measured in vacuum before annealing. Circles represent the devices measured after annealing. (b) Graphene resistance vs. device area.
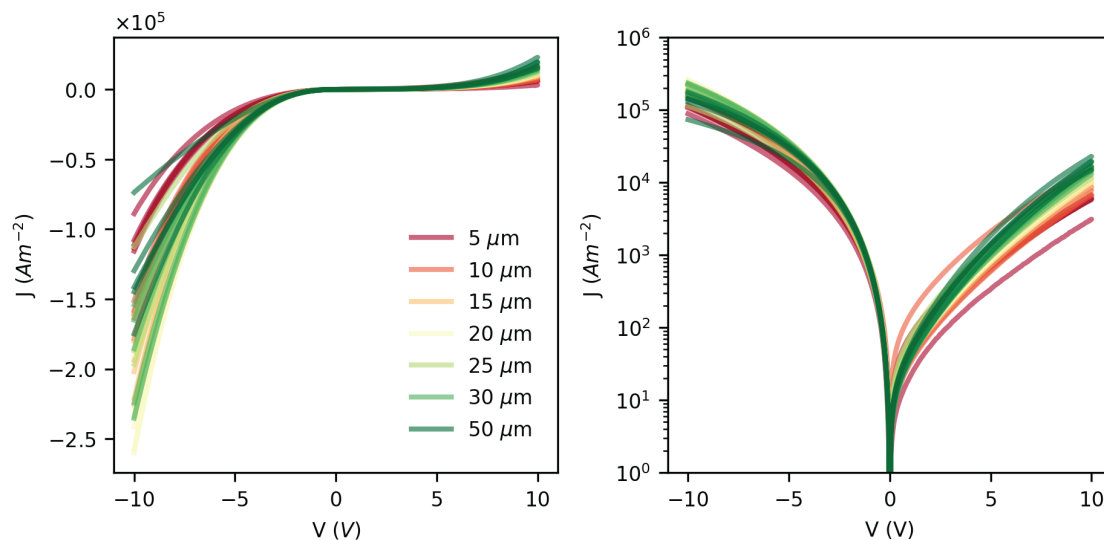

Figure 45: J-Vs of five devices per area of the vertical Au/P3HT/Gr devices measured in vacuum after annealing.
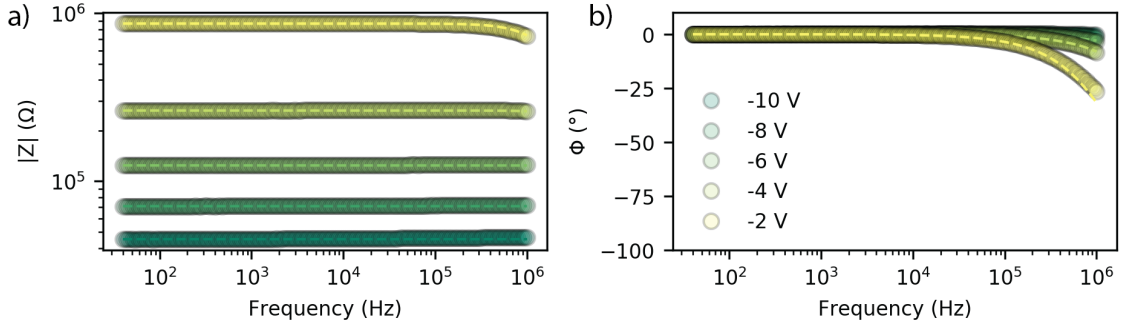
Figure 46: Impedance analysis. Modulus (a) and phase (b) of a representative 20 μm device for negative applied bias. The R//C system cut off frequency shifts above 1 MHz for negative applied bias, where the resistance drops and becomes comparable to the graphene series resistance.

The dielectric constant ϵ_r of P3HT for different devices is calculated using the parallel plate capacitor equation (Eq. S1). The results are shown in Table 1.

$$C = \epsilon_0 \epsilon_r \frac{A}{t} \tag{21}$$

Where ϵ_0 is the vacuum permittivity, A is the device area and t the device thickness. The propagation errors at first order is calculates as shown in Eq. S2.

$$\Delta \epsilon_r = \frac{1}{\epsilon_0} \sqrt{\left(\frac{t}{A}\Delta C\right)^2 + \left(\frac{C}{A}\Delta t\right)^2 + \left(\frac{Ct}{A^2}\Delta A\right)^2} \tag{22}$$

Where ΔC is the fit error, $\Delta t = 30\,\text{nm}$ is the estimation of the thickness error and $\Delta A = \pi((d_{Au} - d_{Gr})/2)^2$ is the estimation of the area error. Where d_{Au} and d_{Gr} are the diameter of the gold and graphene electrodes, respectively.
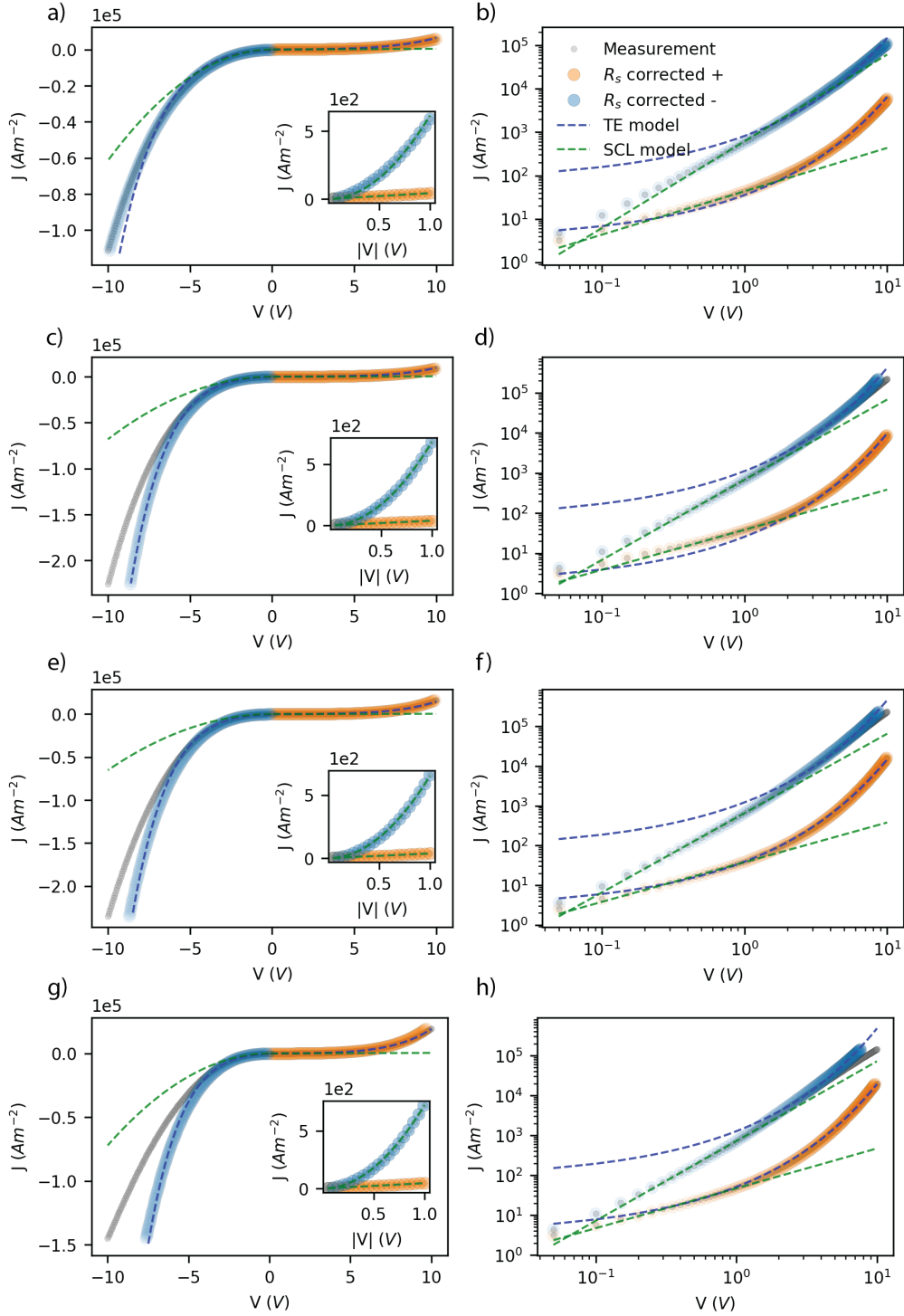
Figure 47: SCL and TE models fitting for different device with diameters: (a-b) 5 μm, (c-d) 15 μm, (e-f) 25 μm, and (g-h) 50 μm. Table 2 shows the statistic of fitting parameters. (a-b) In Fig. 42, one can observe a slightly thicker organic layer around the edge of the devices active area. The latter could have affect the actual average thickness of small devices. To take this effect into account, the thickness of the 5 μm and 10 μm device was set to 130 nm and 120 nm. For all the other devices, where the edge area can be neglected compared to the whole device area, the thickness was set to 100 nm.

A** (Am-2K-2)		Φ (eV)	
Gr/P3HT	Au/P3HT	Gr/P3HT	Au/P3HT
2	18	0.29	0.25
2	22	0.29	0.25
7	18	0.32	0.25
7	22	0.32	0.25

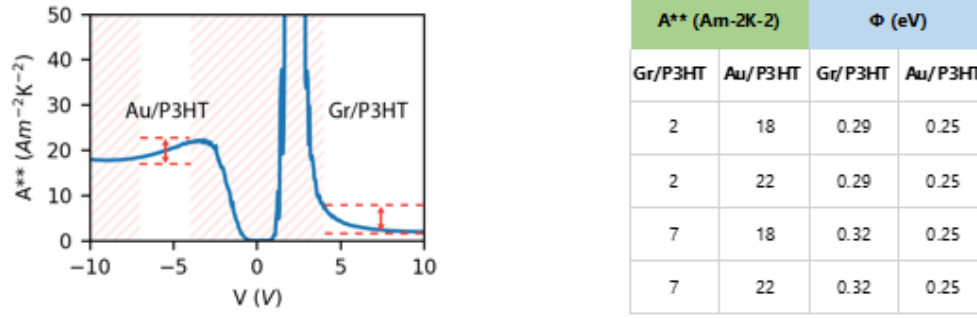Figure 48: (Left) A^{**} as a function of voltage extracted from temperature dependent IV measurements on the representative $5\,\mu m$ device. A^{**} in the range from $-10\,V$ to $-7\,V$ is neglected because of the graphene series resistance. Similarly, A^{**} in the range from $-4\,V$ to $4\,V$ is also neglected because of instrumentation sensitivity. (Right) Potential barrier height calculated for A^{**} values spanning the whole range (ca. $18\,Am^{-2}K^{-2}$ to $22\,Am^{-2}K^{-2}$ for Au / P3HT and $2\,Am^{-2}K^{-2}$ to $7\,Am^{-2}K^{-2}$ for Gr / P3HT).
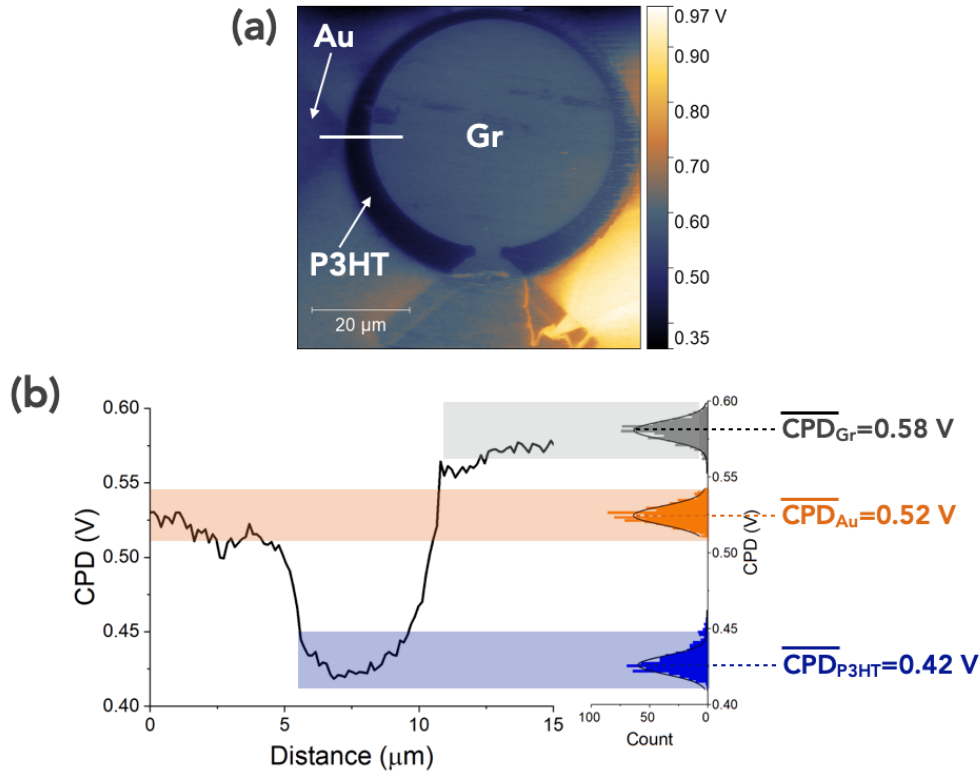
Kelvin Probe Force Microscopy (KPFM)

Figure 49: (a) CPD image of a 50 μm device with the different parts (bottom Au electrode, P3HT film and top graphene electrode) indicated. (b) CPD profile along the white line shown in (a) and histograms of the CPD values measured on Au, Gr and P3HT. The black lines are the fits with a Gaussian distribution, the mean CPD values are given in the figure (FWHM of 14 meV in all cases).

Figure 49a shows a CPD image of a 50 μm device, where the top Gr electrode, the P3HT and the bottom Au electrode are clearly distinguishable. A CPD profile along the white line shown in Figure 49a reveals (Figure 49b) the variations of the CPD for the Au electrode, the P3HT film and the graphene electrode. CPD histograms recorded locally on the Au, P3HT and Gr are shown in the right panel of Figure 49b. Therefore, the deduced potential barrier at the interfaces are $\Phi_{B,Au/P3HT} = 0.10 \pm 0.13$ eV and $\Phi_{B,Gr/P3HT} = 0.16 \pm 0.13$ eV. These values show a similar trend as obtained from the I-V measurements $\Phi_{B,Gr/P3HT} > \phi_{B,Au/P3HT}$ with the same built-in potential (60 meV). However, the KPFM barrier heights are smaller. This can be ascribed to the fact that the I-V measurements were done in vacuum after annealing. In this latter case, the obtained potential barriers at the interfaces are larger than the ones obtained from KPFM measurements done in air and ambient condition.

Chip overview

	A	B	C	D	E	F	G	H	I	J	K	GE diam.	ME diam.
A	AA	AB	AC	AD	AE	AF	AG	AH	AI	AJ	AK	5	7
B	BA	BB	BC	BD	BE	BF	BG	BH	BI	BJ	BK	5	7
C	CA	CB	CC	CD	CE	CF	CG	CH	CI	CJ	CK	5	7
D	DA	DB	DC	DD	DE	DF	DG	DH	DI	DJ	DK	10	12
E	EA	EB	EC	ED	EE	EF	EG	EH	EI	EJ	EK	10	12
F	FA	FB	FC	FD	FE	FF	FG	FH	FI	FJ	FK	15	17
G	GA	GB	GC	GD	GE	GF	GG	GH	GI	GJ	GK	15	17
H	HA	HB	HC	HD	HE	HF	HG	HH	HI	HJ	HK	20	22
I	IA	IB	IC	ID	IE	IF	IG	IH	II	IJ	IK	20	22
J	JA	JB	JC	JD	JE	JF	JG	JH	JI	JJ	JK	20	22
K	KA	KB	KC	KD	KE	KF	KG	KH	KI	KJ	KK	25	27
L	LA	LB	LC	LD	LE	LF	LG	LH	LI	LJ	LK	25	27
M	MA	MB	MC	MD	ME	MF	MG	MH	MI	MJ	MK	30	32
N	NA	NB	NC	ND	NE	NF	NG	NH	NI	NJ	NK	30	32
O	OA	OB	OC	OD	OE	OF	OG	OH	OI	OJ	OK	50	52
P	PA	PB	PC	PD	PE	PF	PG	PH	PI	PJ	PK	50	52
Q	QA	QB	QC	QD	QE	QF	QG	QH	QI	QJ	QK	50	52
Type	Open	Short	Stack	Stack	Stack	Stack	Stack	Stack	Stack	Bridge	Bridge		

Figure 50: Overview of the entire chip. Green cases show the working devices, while the red cases are the not working ones. Roughly, 50% of the chip devices are working and show the same J-V behavior of the device shown in Fig 22.

Space-charge limited (SCL) current modeling

The analytical solution of the Space-Charge-Limited (SCL) current is here reported for convenience, as proposed in previous works.[150, 158, 159, 199]

1. From the continuity equation:

$$J = qn\mu E(x) + qD\frac{dn}{dx} \tag{23}$$

   and the Poisson equation:

$$\frac{d}{dx}E(x) = -\frac{q}{\epsilon}n(x) \tag{24}$$

2. Assuming that the diffusion current is negligible:[199]

$$J = qn\mu E(x) = -\epsilon\mu E(X)\frac{dE(x)}{dx} \tag{25}$$

3. Integrating Eq. 24:

$$\int_0^x J d\theta = J \int_0^x d\theta = \epsilon\mu \int_0^x E(\theta)\frac{dE(\theta)}{d\theta}d\theta$$
$$Jx + K = \frac{1}{2}\epsilon\mu E(x)^2 \tag{26}$$

   where K is a constant.

4. Solving Eq. 26 for the electrical field $E(x)$:

$$E(x) = \sqrt{\frac{2J}{\epsilon\mu}(x + K')} \tag{27}$$

where $K' = \frac{K}{J}$.

5. K' is found using the boundary conditions at the injecting contact ($x = 0$). Defining $n|_{x=0} = N_0$ and applying the Dirichlet boundary condition $\frac{dE(x)}{dx}\Big|_{x=0} = \frac{qN_0}{\epsilon}$, K' is

$$K' = \frac{J\epsilon}{2\mu N_0^2 q^2} \tag{28}$$

6. Then, plugging K' in Eq. 27:

$$E(x) = \sqrt{\frac{2J}{\epsilon\mu}\left(x + \frac{J\epsilon}{2\mu N_0^2 q^2}\right)}$$

$$E(0) = \sqrt{\frac{J^2}{\mu^2 N_0^2 q^2}} = \frac{J}{\mu N_0 q} \tag{29}$$

7. Finally, the voltage associated to the current J in the semiconductor of length L is given by:

$$V = -\int_0^L E(X)dx = \sqrt{\frac{8J}{9\epsilon\mu}}\left[(L + K')^{3/2} + K'^{3/2}\right] \tag{30}$$

8. The current-voltage relation is found solving Eq. 30 for the current. Two solutions are found:

$$\begin{aligned} J &= \frac{9}{8}\epsilon\mu\frac{V^2}{L^3} &&\text{for} \quad K' \ll L \\ J &= q\mu N_0\frac{V}{L} &&\text{for} \quad K' \gg L \end{aligned} \tag{31}$$

J is the current density driven through the device by applying the bias V. The other parameters are defined by the semiconductor properties. N_0, that is the charge carrier density at the interface, is defined by the density of states of the semiconductor N_{DOS} and by the potential barrier height Φ_B at the interface:

$$n|_{x=0} = N_0 = N_{DOS}\exp\left(-\frac{E_{HOMO} - \Phi_M}{kT}\right) = N_{DOS}\exp\left(-\frac{\Phi_B}{kT}\right) \tag{32}$$

The case of a 20 μm representative device shown in Fig. 22 is considered. N_0 at the Gr/P3HT interface can be measured by (i) extracting the hole mobility of P3HT using Eq. 31 ($K' \ll L$) for negative biases and (ii) applying Eq. 31 ($K' \gg L$)

in the linear region for positive biases. The obtained charge carrier density at the Gr/P3HT interface is $N_0 = 1.1 \times 10^{15}\,\mathrm{cm}^{-3}$.

Then, using the potential barrier height (0.31 eV, extracted from TE model) and N_0 at the Gr/P3HT interface, N_{DOS} of P3HT can be calculated: $N_{DOS} = 2.4 \times 10^{20}\,\mathrm{cm}^{-3}$. Finally, N_0 at the Au/P3HT can be computed using Eq. 31 ($K' \ll L$) and the potential barrier height (0.25 eV). Obtained charge carrier density at the Au/P3HT interface is $N_0 = 1.2 \times 10^{16}\,\mathrm{cm}^{-3}$. It is worth observing that the image-charge induced lowering of potential barrier is not considered. N_0 may depend on the applied bias and be larger than the estimated value1 . Figure 51 shows K' vs. J, i.e. the charge carrier density and the electrical field across the stack for the two different boundary conditions
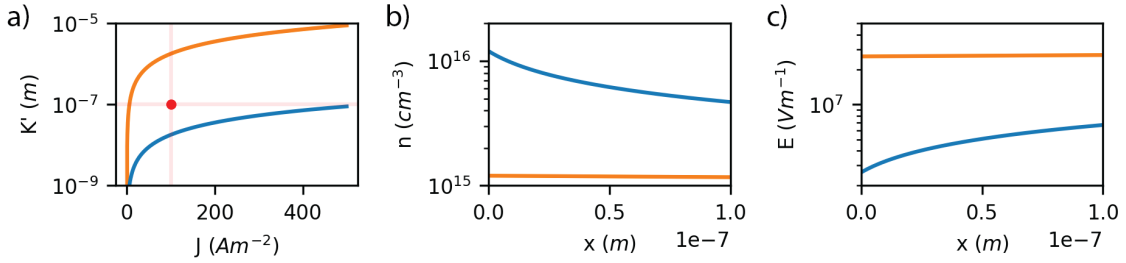

Figure 51: Space-charge limited current model calculated in the current density range of the measured devices. (a) K' vs. J showing the two different solution of the space-charge limited current model (Eq. 29 and 30). The horizontal red line shows $L = 100\,\mathrm{nm}$ of Eq. 28. Orange line corresponds to $N_0 = 1.1 \times 10^{15}\,\mathrm{cm}^{-3}$ ($K' > L$) and blue line to $N_0 = 1.2 \times 10^{16}\,\mathrm{cm}^{-3}$ ($K' < L$). The vertical red line show the current density used to calculate $n(x)$ and $E(x)$ of plot (b) and (c). (b) Charge carrier density (b) and electrical field (c) across the across the vertical for a current density $J = 100\,\mathrm{Am}^{-2}$.

E   Charge transport across Au-C60-Gr
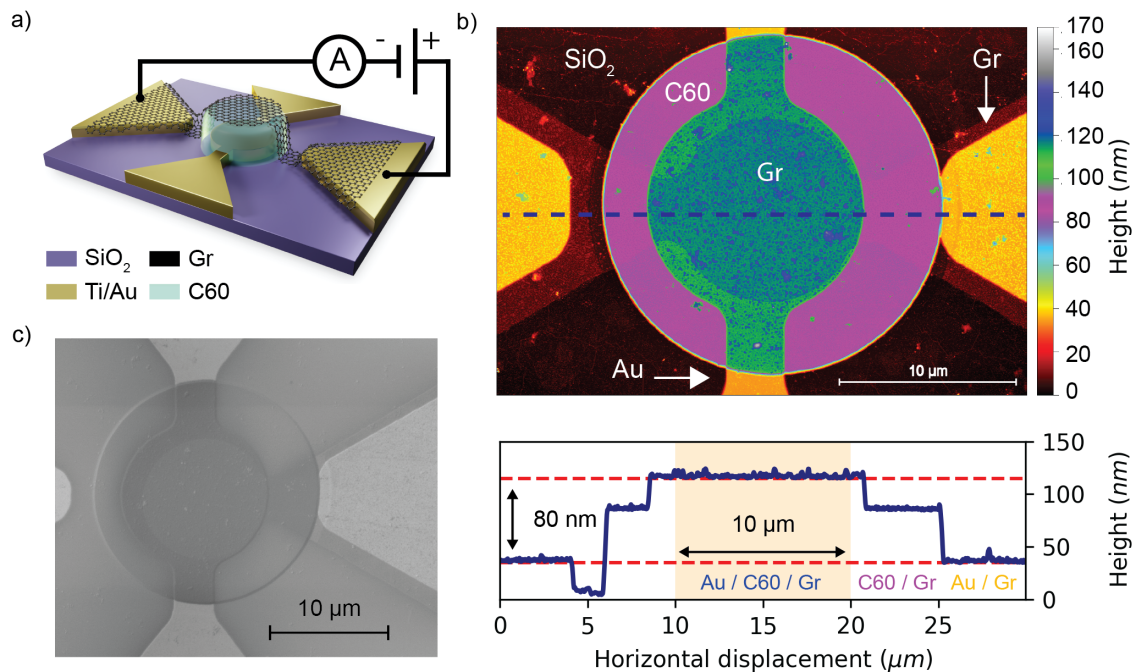
FIB/SEM/AFM characterization

Figure 52: (a) 3D schematic of a representative 10 µm Graphene Bridge device (not to scale). Adapted from Oswald, J. et al. ACS Appl. Mater. Interfaces 2022.1 (b) AFM height image and profile of a representative 10 µm bridge device. (c) SEM image of a representative 10 µm Au / C60 / Gr Vertical Stack device.
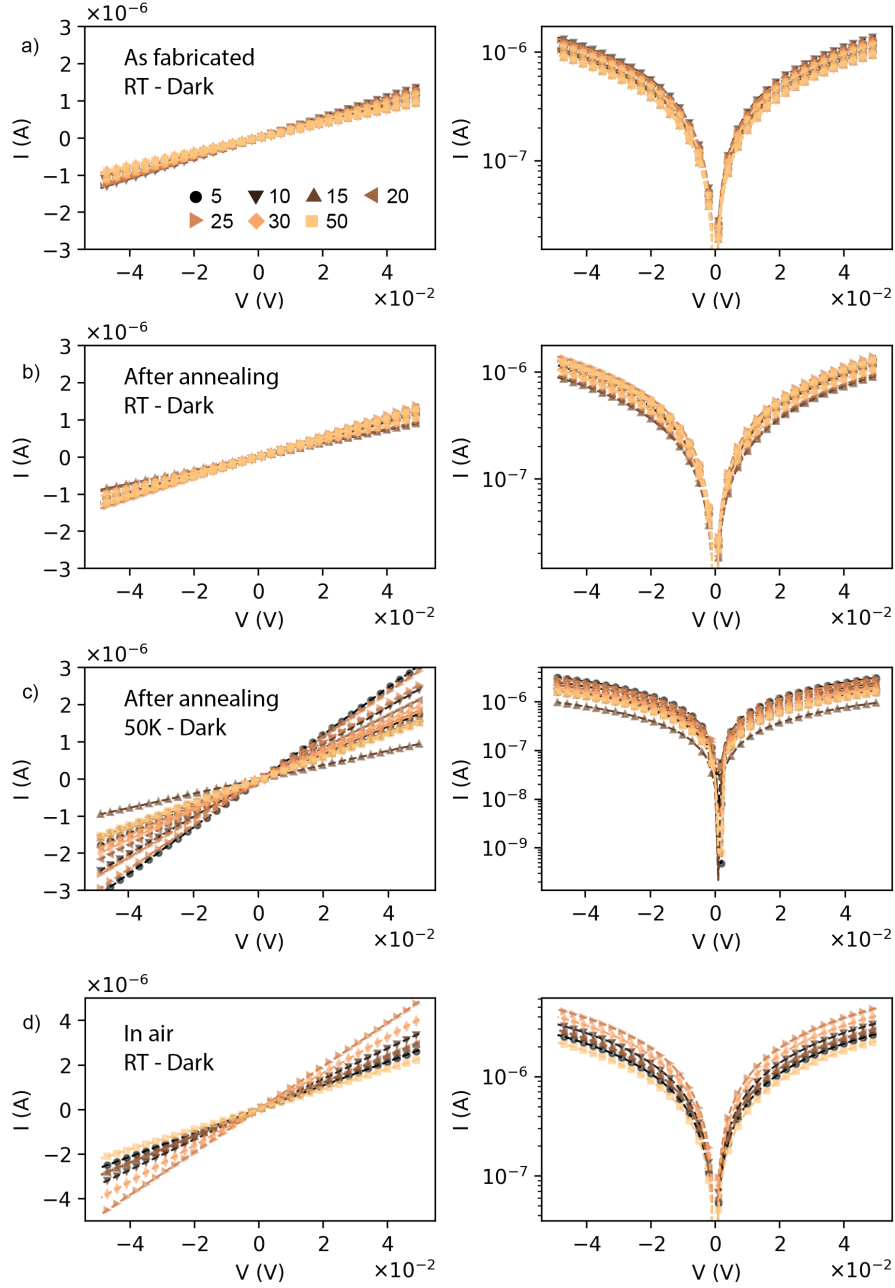
Electrical characterization

Figure 53: Electrical measurements of the Graphene Bridges under different conditions. Left: linear scale. Right: log scale. Symbols represent the diameter of the device. (a) I-V traces of the devices as fabricated measured under vacuum ($\approx 1 \times 10^{-6}$ mbar), at room temperature (293 K) and in dark. (b) I-V traces of the devices after annealing (110 °C for 12 h, 1×10^{-6} mbar) measured under vacuum (1×10^{-6} mbar), at room temperature (293 K), and in dark. (c) I-V traces of the devices after annealing measured under vacuum 1×10^{-6} mbar), at 50 K, and in dark. (d) I-V traces of the devices exposed to air. The graphene resistance for a representative device for each diameter, extracted from the linear fit of the I-V traces, is given in Table 5.

Device (μm)	As fabricated (1×10^{-6} mbar)	After annealing (1×10^{-6} mbar, 12 h 110 °C)		In air
	RT - 293 K, Dark	RT - 293 K, Dark	$T = 50$ K, Dark	RT - 293 K, Dark
5	42213	42137	27726	18790
10	42178	40434	20162	14720
15	40343	40536	30875	16718
20	41677	41384	22879	16676
25	36988	38531	19245	10367
30	51914	46965	24877	12350
50	52795	46765	31218	22197

Table 5: Graphene resistance (measured in Ω) of a representative Graphene Bridge device for each size measured under different environment conditions. Similar resistances are measured for graphene at room temperature (293 K) in dark, and after annealing (110 °C for 12 h) in dark. Lower resistance is found at low temperature (50 K), possibly due to higher charge mobility, and in air conditions (293 K in dark), as expected from an increased charge carrier density due to the O_2 and H_{20} p-doping of graphene. Under all conditions, the resistance of the Graphene Bridge is lower than the one of the Vertical Stack. Therefore, the series resistance R_S shown in the circuit of Figure 26 can be neglected, and the current across the Vertical Stack is limited by the interfaces.
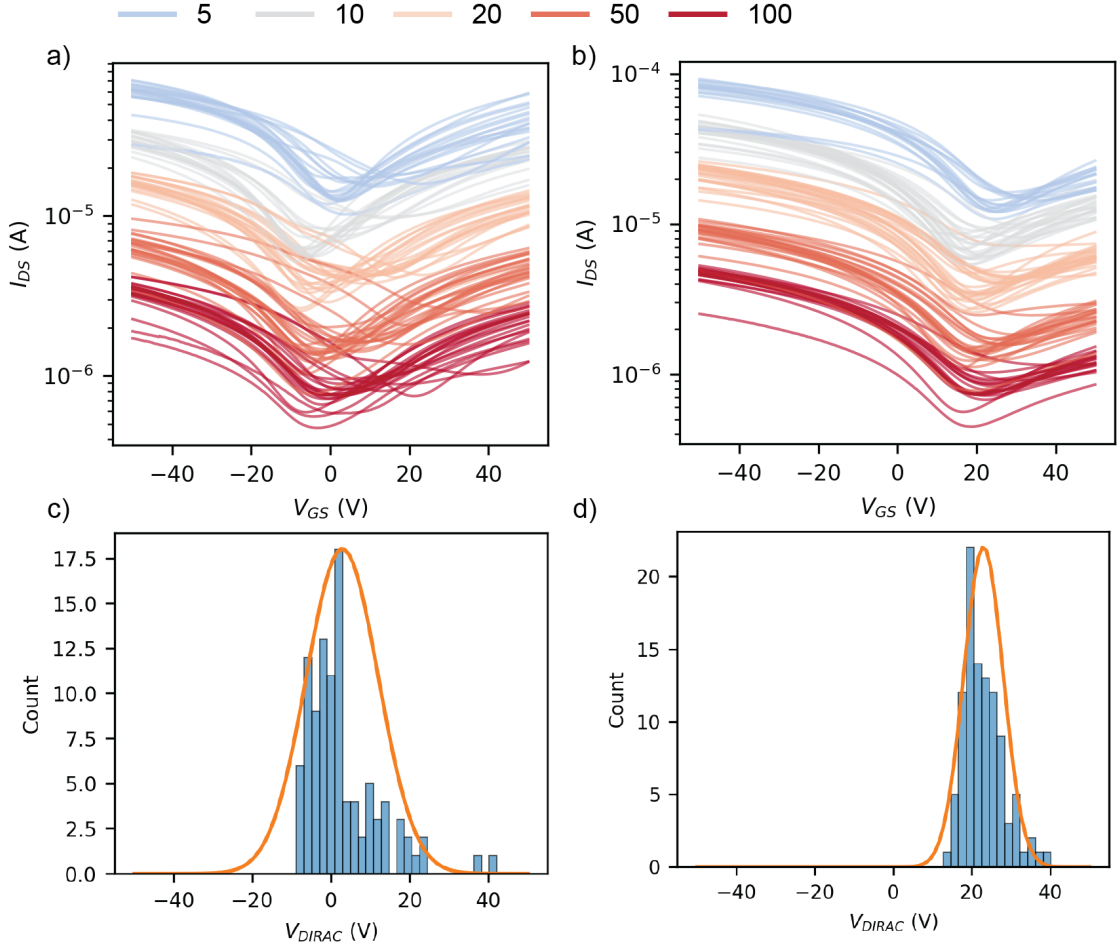
Figure 54: Electrical measurements of graphene field effect transistors under vacuum ($\approx 1 \times 10^{-6}$ mbar) at room temperature (293 K). Channel length is 5 µm while the lengths of the devices are 5, 10, 20, 50 and 100 µm, as shown by the colored lines of (a) and (b). (a) I_{ds} vs. V_{gs} characteristics of pristine graphene field effect transistors. (b) I_{ds} vs. V_{gs} characteristics of the graphene field effect transistor doped by C60 (5 nm thin film evaporated on top).

Induced charge carrier density in graphene due to C60

The induced charge carrier density in graphene is deduced from a parallel plate capacitor model, in formula

$$n = C_{gs} \frac{V_{dirac} - V_{gs}}{q} \tag{33}$$

Eq. S1 Where $C_{gs} = (\epsilon_0 \epsilon_r)/t$ is the capacitance per unit area, t is the thickness of the oxide (300 nm) and ϵ_r is the dielectric constant of SiO$_2$ (ca. 3.9). Since the charge neutrality point is shifted by roughly 20 V, as shown in Fig. 54, the induced charge density of graphene doped by C60 is ca. $n \approx 1.4 \times 10^{12}$ cm^{-2}.
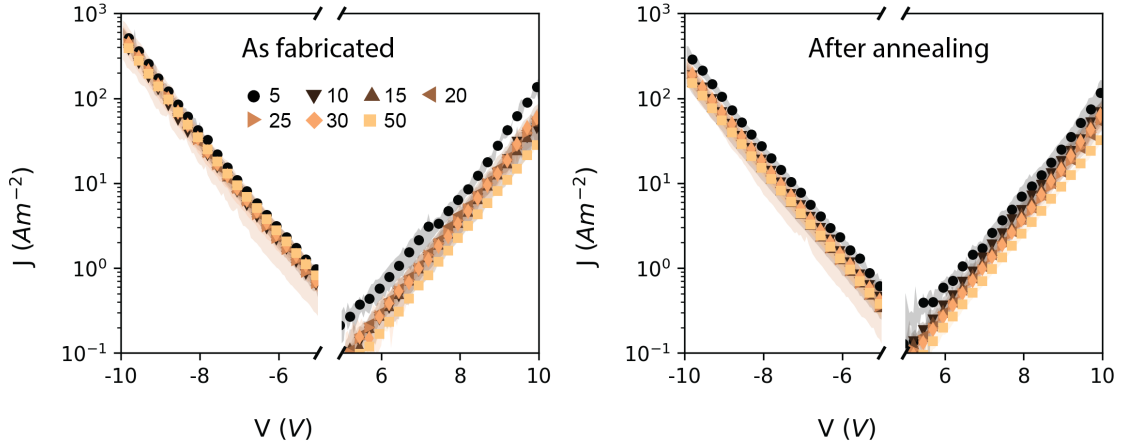
Figure 55: Effect of annealing under vacuum (1×10^{-6} mbar) on electrical transport across the Vertical Stack. (a) J-V traces of the as fabricated devices measured under vacuum (1×10^{-6} mbar) at room temperature (293 K). (b) J-V traces measured in vacuum at room temperature, after annealing at 110 °C for 12 h. The graphs show the average of the current-voltage characteristics measured on 2 devices for each diameter: 5, 10, 15, 20, 25, 30, and 50 µm.
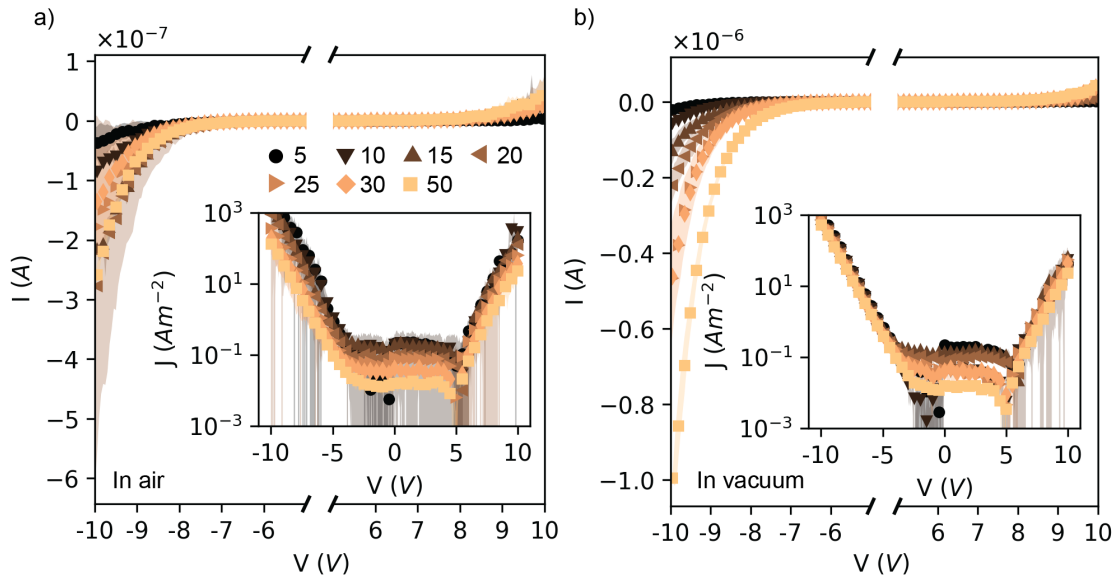

Figure 56: Effect of the environment conditions on the I-V traces of the Vertical Stack. (a) Electrical measurements in air at room temperature (293 K). (b) Electrical measurements under vacuum ($\approx 1 \times 10^{-6}$ mbar) at room temperature (293 K). (a) and (b) are measured on the same set of devices. The graphs show the average of the current-voltage characteristics measured on 2 devices for each diameter: 5, 10, 15, 20, 25, 30, and 50 µm.
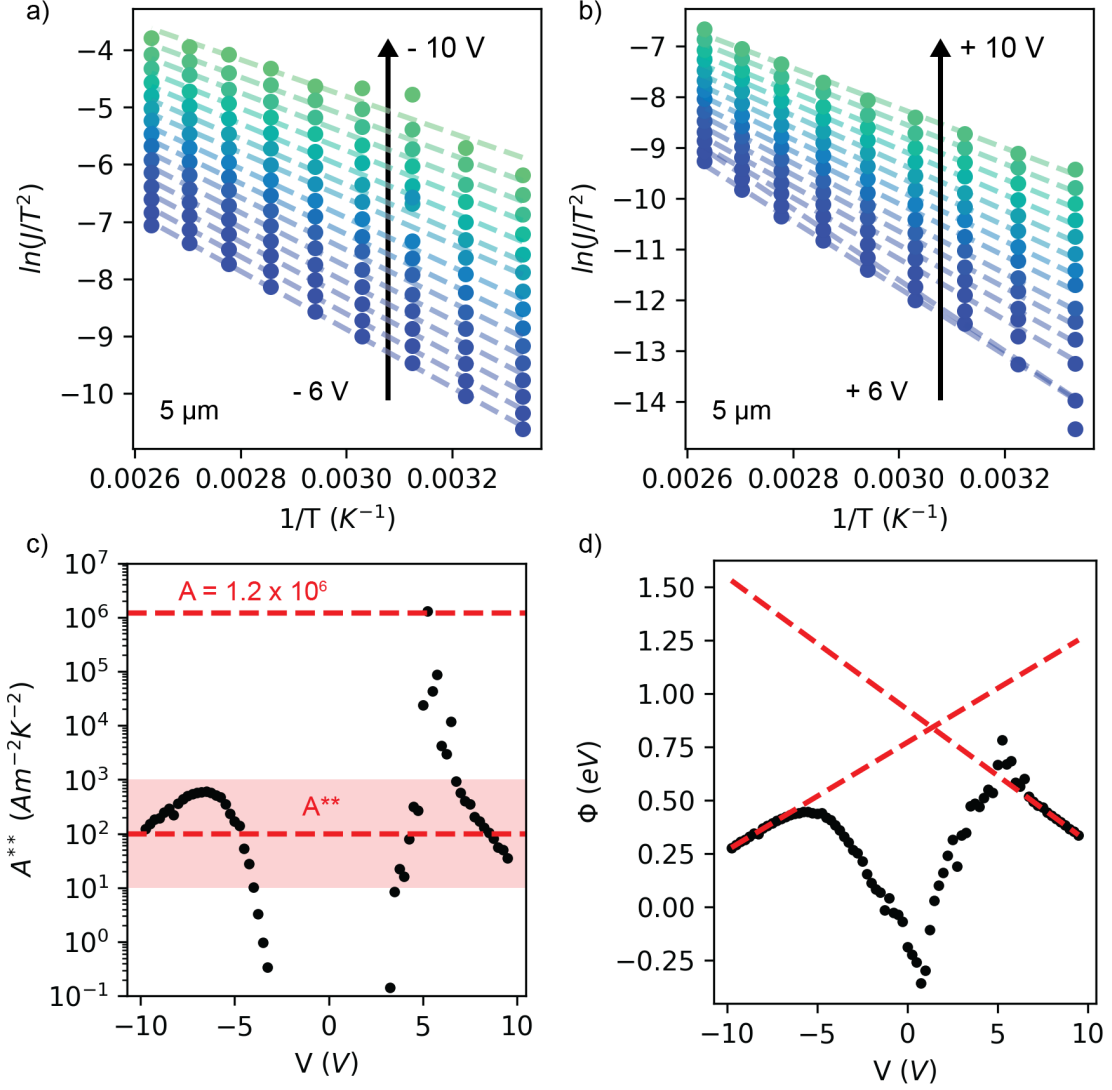
Figure 57: Richardson plot (of the non-ideal Schottky diode model, i.e. $ln(J/T^2) = ln(A^{**}_{1,2}) - \Phi_{1,2}(V)/kT$ of a representative $50\,\mu m$ device for (a) negative applied bias and (b) positive applied bias. For $V < 0$, the equation represent the reverse current of SB_1 and for $V > 0$ the equation represent the reverse current of SB_2. In this model the individual interface is considered. (c) Effective Richardson constant $A^{**}_{1,2}$ extracted from the intercept $ln(A^{**}_{1,2})$ of the Richardson plots, for negative (a) and positive (b) voltages. (d) Potential barrier height as a function of bias $\Phi_{1,2}(V)$, extracted from the $slope - \Phi_{1,2}(V)/k$ of the Richardson plot, for negative (a) and positive (b) voltages. The nominal barrier heights $\Phi_{01,2}$ and ideality factors $n_{1,2}$ are extracted from the intercept and slope of the linear fit of $\Phi_{1,2}(V)$, respectively. Table 6 shows the resulting $\Phi_{01,2}$ and $n_{1,2}$.
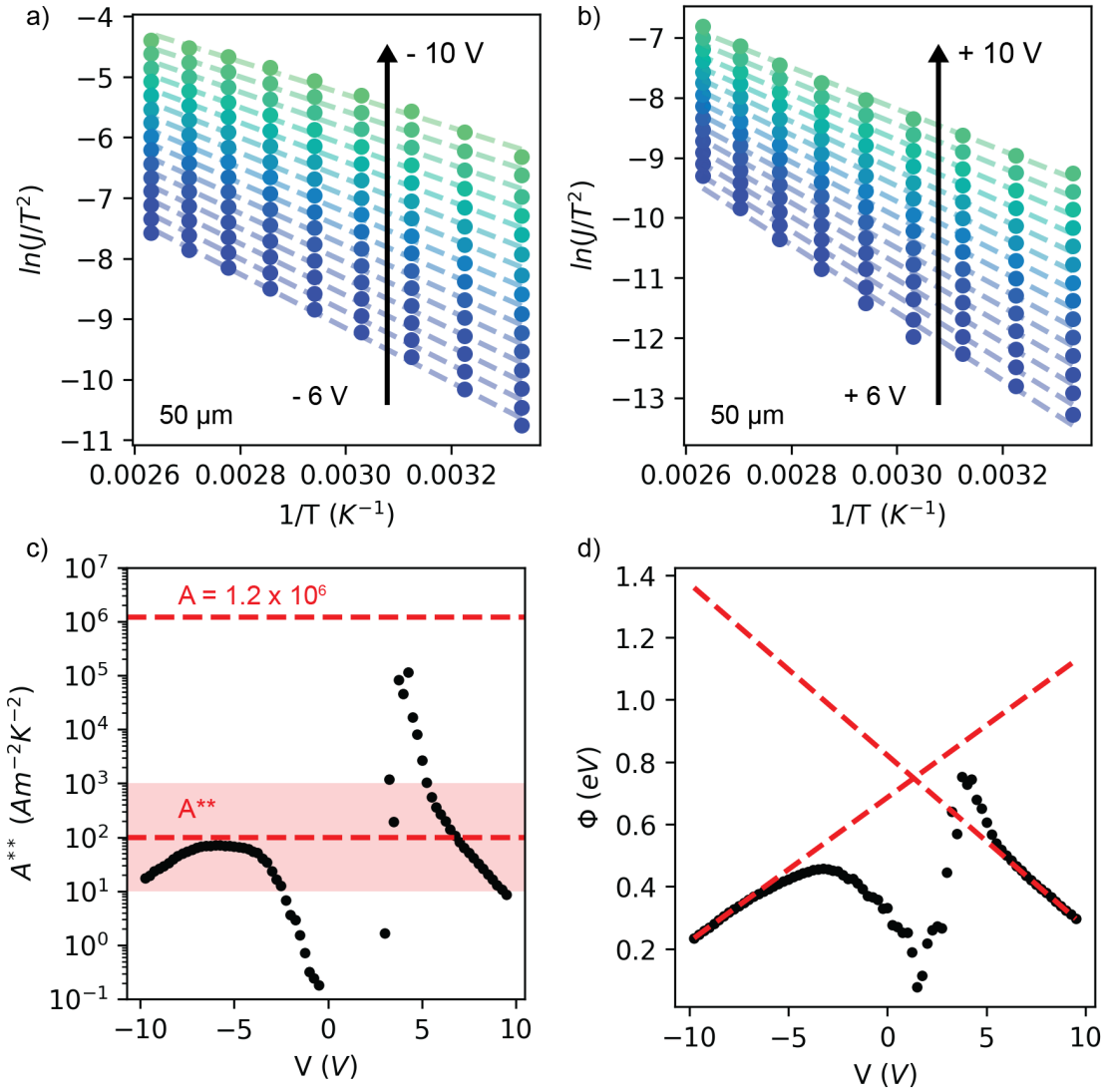
Figure 58: Richardson plot (of the non-ideal Schottky diode model, i.e. $ln(J/T^2) = ln(A_{1,2}^{**}) - \Phi_{1,2}(V)/kT$ of a representative 5 μm device for (a) negative applied bias and (b) positive applied bias. For $V < 0$, the equation represent the reverse current of SB_1 and for $V > 0$ the equation represent the reverse current of SB_2. In this model the individual interface is considered. (c) Effective Richardson constant $A_{1,2}^{**}$ extracted from the intercept $ln(A_{1,2}^{**})$ of the Richardson plots, for negative (a) and positive (b) voltages. (d) Potential barrier height as a function of bias $\Phi_{1,2}(V)$, extracted from the $slope - \Phi_{1,2}(V)/k$ of the Richardson plot, for negative (a) and positive (b) voltages. The nominal barrier heights $\Phi_{01,2}$ and ideality factors $n_{1,2}$ are extracted from the intercept and slope of the linear fit of $\Phi_{1,2}(V)$, respectively. Table 6 shows the resulting $\Phi_{01,2}$ and $n_{1,2}$
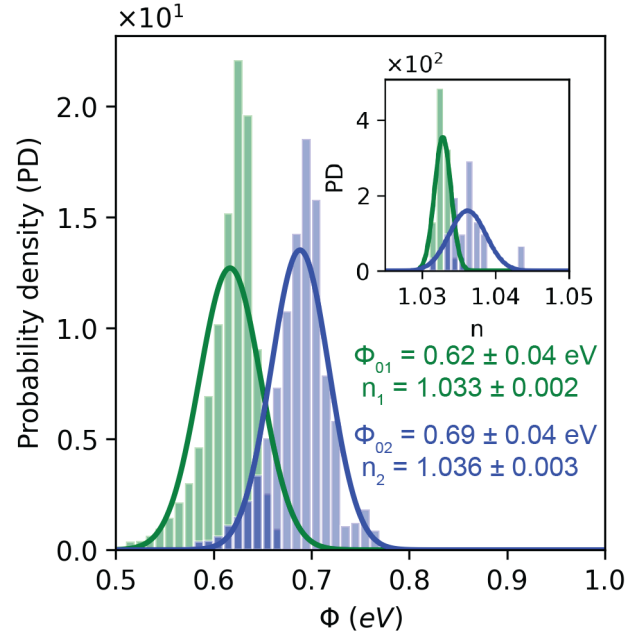
Figure 59: Distribution of $\Phi_{01,02}$ and $n_{1,2}$ extracted from the DSB on 35 device (5 devices for each diameter), associated to the Gr / C60 and Au / C60 interfaces, respectively. Each individual I-V shown in Fig. 60, was fitted using various values of the effective Richardson constant A^{**} varying in the range $1 \times 10^1 \, \mathrm{Am}^{-2}\mathrm{K}^{-1}$ to $1 \times 10^3 \, \mathrm{Am}^{-2}\mathrm{K}^{-1}$ (in steps of $10 \, \mathrm{Am}^{-2}\mathrm{K}^{-1}$). The extracted energy barrier heights were used to construct the histogram. The variation of the energy barriers extracted with different A^{**} from the aforementioned range is less than $0.1 \, \mathrm{eV}$ compared to the energy barriers extracted using $A^{**} = 100 \, \mathrm{Am}^{-2}\mathrm{K}^{-1}$ and showed in Fig. 24b.

Discussion on the non-ideal Schottky diode model fitting of individual interfaces (SB_1 and SB_2)

Table 6 shows the ideality factors and energy barriers of SB_1 and SB_2 obtained from the Richardson plots (Fig. 57 and Fig. 58) and considering the non-ideal Schottky diode model with ideality factor n. The resulting effective Richardson constant A^{**} is voltage dependent and vary in the range $1 \times 10^1 \, \mathrm{Am}^{-2}\mathrm{K}^{-1}$ to $1 \times 10^3 \, \mathrm{Am}^{-2}\mathrm{K}^{-1}$ for $|V| > 5V$. The energy barrier and ideality factor of SB1 are smaller than SB_2 (i.e. $\Phi_01 < \Phi_2$ and $n_1 < n_2$), following the same trend observed for the results of the DSB model. The higher ideality factors $n_{1,2}$ obtained from the individual Schottky diode model is possibly due to the presence of the second energy barrier and/or to the voltage dependent Richardson constants. This could also lead to a slight overestimation of the energy barriers $\Phi_{01,2}$. For this reason, in the DSB model presented in Figure 2, the Richardson constant was set to the fixed value of $A^{**} = 100 \, \mathrm{Am}^{-2}\mathrm{K}^{-1}$ (red dashed line in Fig. 57 and Fig. 58), and the energy barriers

error induced by the Richardson constant, varying in the range $1 \times 10^1 \, \mathrm{Am^{-2}K^{-1}}$ to $1 \times 10^3 \, \mathrm{Am^{-2}K^{-1}}$ (observed range for the individual Schottky diode model, Fig. 57 and Fig. 58), is below $0.1 \, \mathrm{eV}$, as shown in Figure 59.

Device (μm)	n_1	n_2	Φ_{01} (eV)	Φ_{02} (eV)
50 (Fig. 58)	1.049 ± 0.000	1.058 ± 0.000	0.69 ± 0.00	0.82 ± 0.00
5 (Fig. 57)	1.053 ± 0.002	1.066 ± 0.001	0.77 ± 0.01	0.93 ± 0.00

Table 6: Ideality factors and energy barriers obtained from the Richardson plots of the individual Gr / C60 and Au / C60 interfaces. The data of the 50 µm and 5 µm devices is shown in Fig. 57 and Fig. 58, respectively. The table shows the errors of the linear fit method used to extrapolate the intercept and the slope of the data in Fig. 57-58.
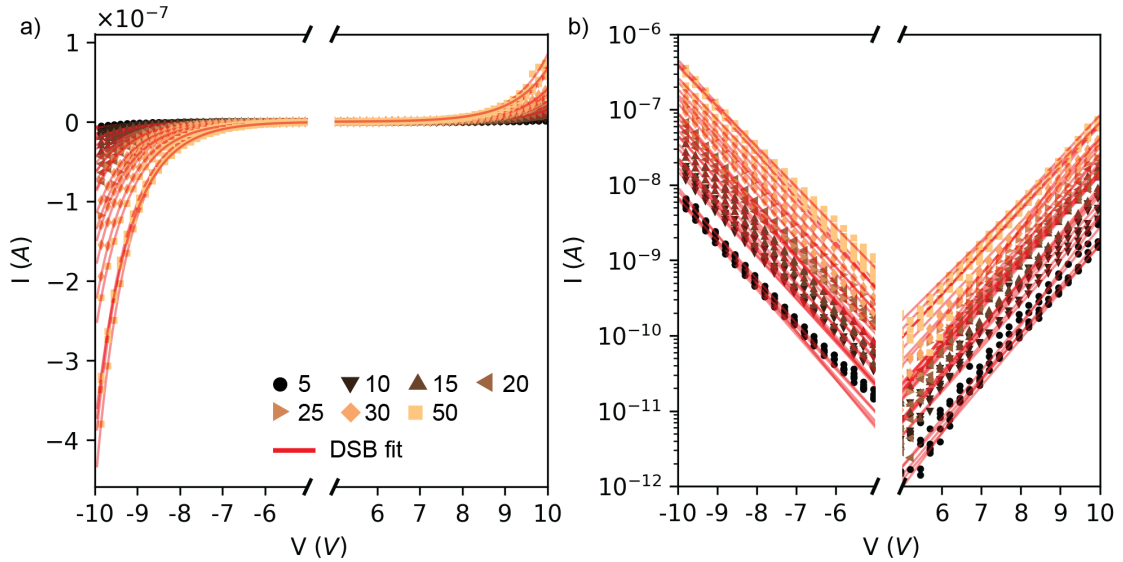

Figure 60: Electrical measurements under vacuum (1×10^{-6} mbar) at room temperature (293 K). (a) I-V traces and DSB model fitting (red dashed lines) of the 35 devices (5 devices for each size). (b) Same I-V traces in log scale. The figure does not display the I-V data in the range from $-5\,\mathrm{V}$ to $5\,\mathrm{V}$, where the current is below the sensitivity of the instrument (see Figure 63).
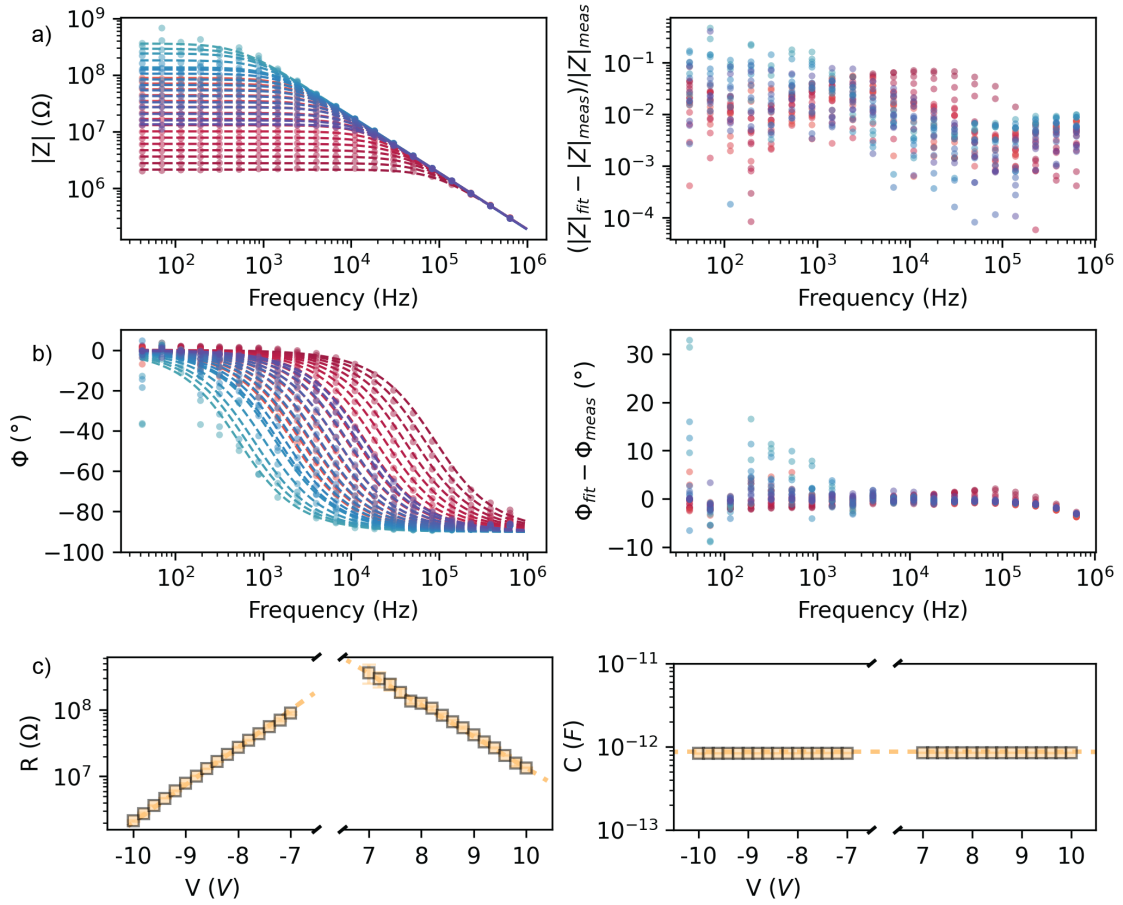
Figure 61: Impedance analysis of a representative 50 μm device. (a) Modulus and $R//C$ model fit (dashed line) of the impedance with relative error. (b) Phase and $R//C$ model fit (dashed line) of the impedance with absolute error. (c) R and C extracted from the fit. The capacitance C is bias independent and therefore, the OSC is fully depleted in the considered voltage range.

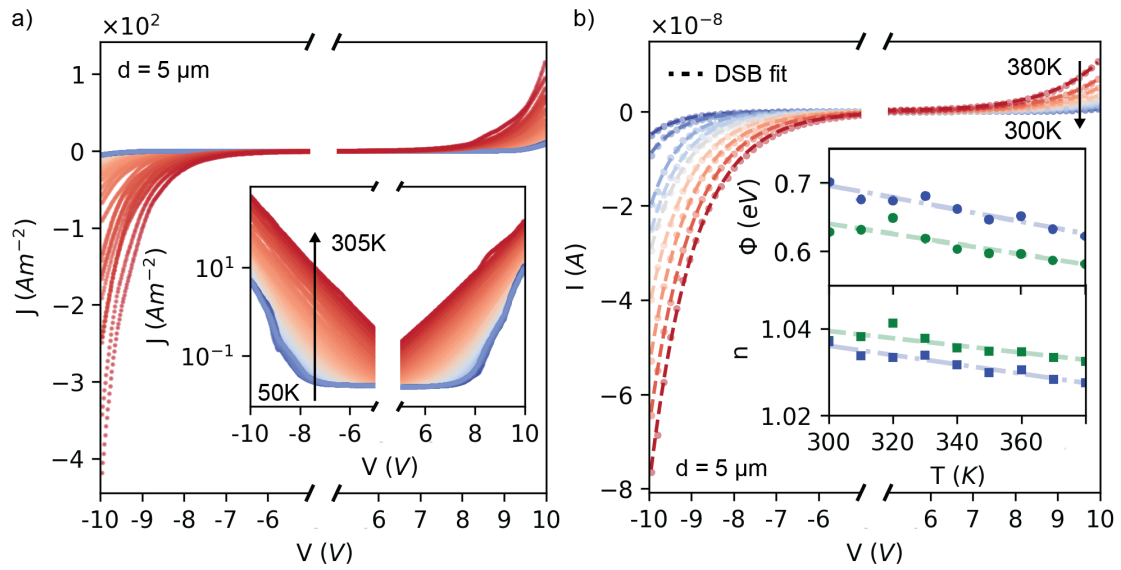Figure 62: (a) Temperature dependent J-V characteristic of a 5 µm device from 50 K to 305 K. The inset shows the same traces in log scale. (b) Temperature dependent I-V characteristic of a representative 5 µm device from 300 K to 380 K in steps of 10 K. The inset shows Φ_{01}, n_1 and Φ_{02}, n_2, extracted from the DSB model, as a function of temperature.
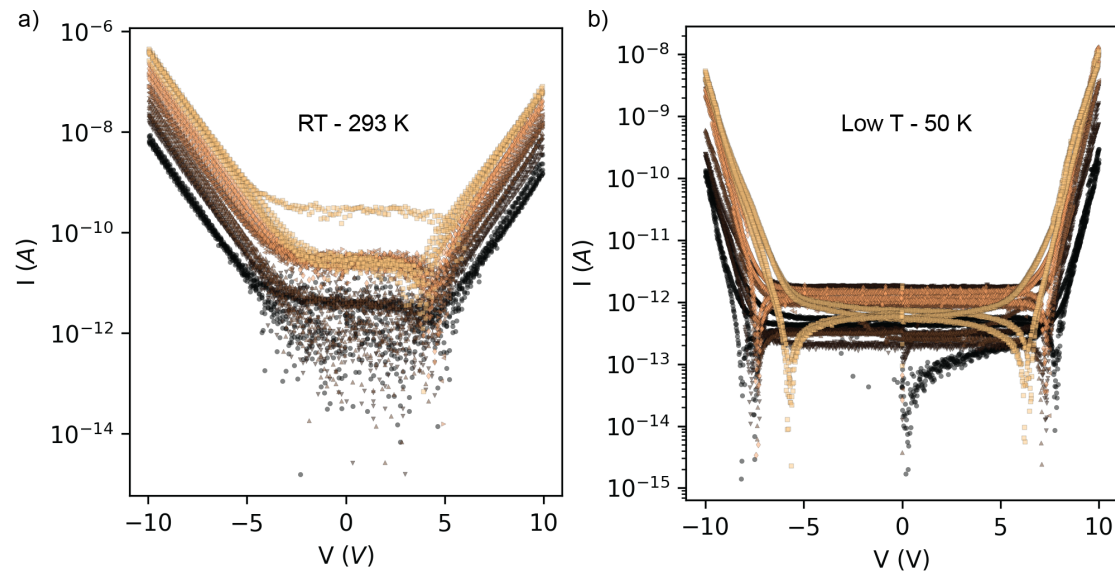
Figure 63: Forward and backward I-V sweeps. (a) I-Vs measured under vacuum at room temperature (293 K) with the Keithley 4200 Semiconductor Parameter Analyzer. The current is below the sensitivity of the instrument in the range from $-5\,\mathrm{V}$ to $5\,\mathrm{V}$. (b) I-Vs measured at low temperature (50 K) Lakeshore probe station (CRX-6.5K) operating under vacuum ($1 \times 10^{-6}\,\mathrm{mbar}$). The I-V sweeps show hysteresis in the range from $-7\,\mathrm{V}$ to $7\,\mathrm{V}$. Forward and backward I-V sweeps are overlapping at higher voltages, where the FN tunneling model is applied.

Chip overview

	A	B	C	D	E	F	G	H	I	J	K	GE diam.	ME diam.
A	AA	AB	AC	AD	AE	AF	AG	AH	AI	AJ	AK	5	7
B	BA	BB	BC	BD	BE	BF	BG	BH	BI	BJ	BK	5	7
C	CA	CB	CC	CD	CE	CF	CG	CH	CI	CJ	CK	5	7
D	DA	DB	DC	DD	DE	DF	DG	DH	DI	DJ	DK	10	12
E	EA	EB	EC	ED	EE	EF	EG	EH	EI	EJ	EK	10	12
F	FA	FB	FC	FD	FE	FF	FG	FH	FI	FJ	FK	15	17
G	GA	GB	GC	GD	GE	GF	GG	GH	GI	GJ	GK	15	17
H	HA	HB	HC	HD	HE	HF	HG	HH	HI	HJ	HK	20	22
I	IA	IB	IC	ID	IE	IF	IG	IH	II	IJ	IK	20	22
J	JA	JB	JC	JD	JE	JF	JG	JH	JI	JJ	JK	20	22
K	KA	KB	KC	KD	KE	KF	KG	KH	KI	KJ	KK	25	27
L	LA	LB	LC	LD	LE	LF	LG	LH	LI	LJ	LK	25	27
M	MA	MB	MC	MD	ME	MF	MG	MH	MI	MJ	MK	30	32
N	NA	NB	NC	ND	NE	NF	NG	NH	NI	NJ	NK	30	32
O	OA	OB	OC	OD	OE	OF	OG	OH	OI	OJ	OK	50	52
P	PA	PB	PC	PD	PE	PF	PG	PH	PI	PJ	PK	50	52
Q	QA	QB	QC	QD	QE	QF	QG	QH	QI	QJ	QK	50	52
Type	Open	Short	Stack	Stack	Stack.	Stack	Stack	Stack	Stack	Bridge	Bridge		

Figure 64: Overview of the entire chip. Green cases show the working devices, while the red cases are the not working ones. Roughly, 50% of the chip devices are working and show the same J-V behavior of the device.

F   Au-Pentacene-Al vertical diodes

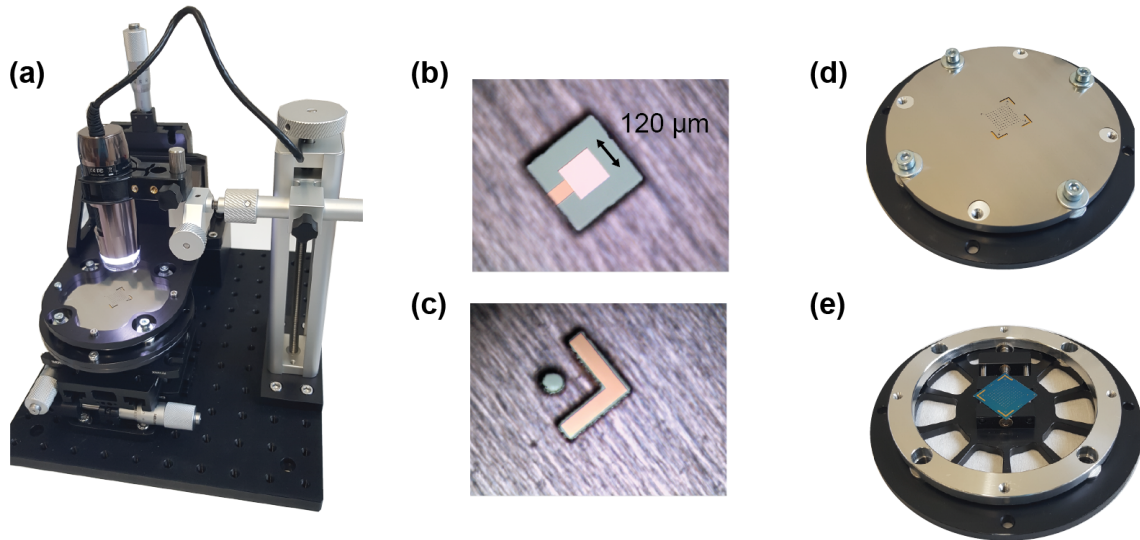## Construction of the metal masks aligner

Figure 65: (a) Photograph of the metal masks aligner. (b) Optical microscope image allowing to align the metal mask to the substrate. (c) The sample and mask alignment markers. (d) Sample and mask holder ready for thermal evaporation. (e) Sample mounted on the holder without the metal mask.

Figure 65a shows the home-built mask aligner. The aligner consist of four micromanipualtor (Thorlabs): two are dedicated to the x- and y-axis movement of the sample with respect to the metal mask, one is used for the in-plane tilt of the sample and one is used to bring the mask in contact with the sample along the z-axis. Figure 65b shows the optical microscope image bottom electrode on the chip aligned with the metal mask used for the evaporation of the OSC. The alignment is possible thaks to the markers (Figure 65b) placed on edges of the mask and sample, and the optical microscope (Dino-Lite) showed in Figure 65a. Once aligned, the mask and sample holders are screwed together, as showed in Figure 65d, and placed into the thermal evaporator. After the thin-film deposition, the two parts are unscrewed and the sample released.

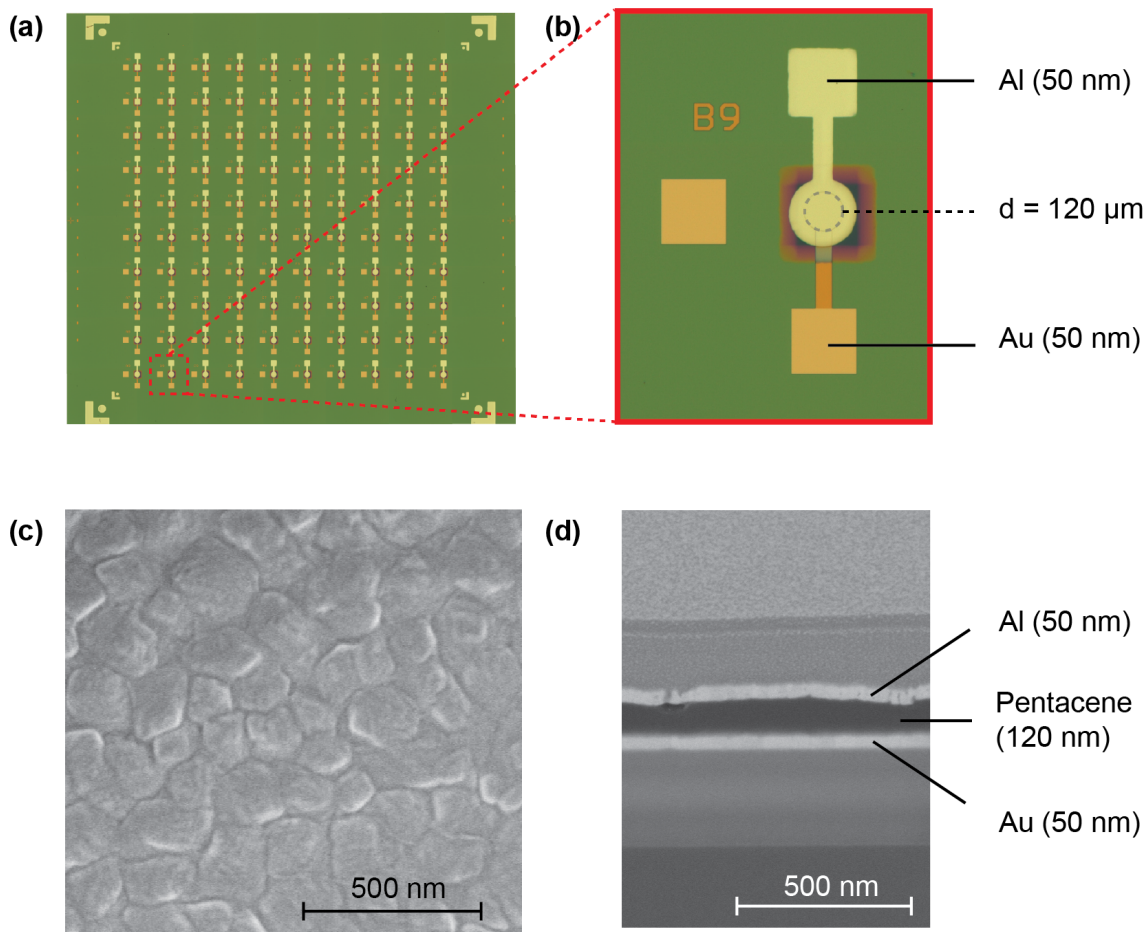## Fabrication of the vertical Au-Pentacene-Al diodes

Figure 66: (a) Optical microscope image of the whole chip. (b) Zoom-in on a representative vertical circular device with radius $r = 60\,\mu m$. (c) SEM image of the surface of the thermally evaporated thin film of Pentacene. (d) SEM cross-section of the Au-Pentacene-Al device.

Figure 66a shows an overview of the Si/SiO$_2$ chip with the vertical Au-Pentance-Al devices. The bottom Ti (5 nm / Au (50 nm) were fabricated by photolithography. The 120 nm thick film of Petacene and the 50 nm Al top electrode are thermally evaporated through metal masks. The chip includes 100 devices, half of which have square shaped electrodes, while the other half have circular electrodes. A representative circular device with diameter $d = 120\,\mu m$ is shown in Figure 66b. The width w and diameter d of the square and circular electrodes are 120, 140, 160, 180 and 200 μm. Figure 66c shows the SEM image of the Pentacene thin film on the Au electrode without the top Al electrode. Figure 66d shows the SEM cross-section of the Au-Pentacene-Al stack deposited on top of a Si/SiO$_2$ substrate. The image shows a uniform 120 nm film of Pentacene sandwiched between 50 nm Al and Au electrodes.
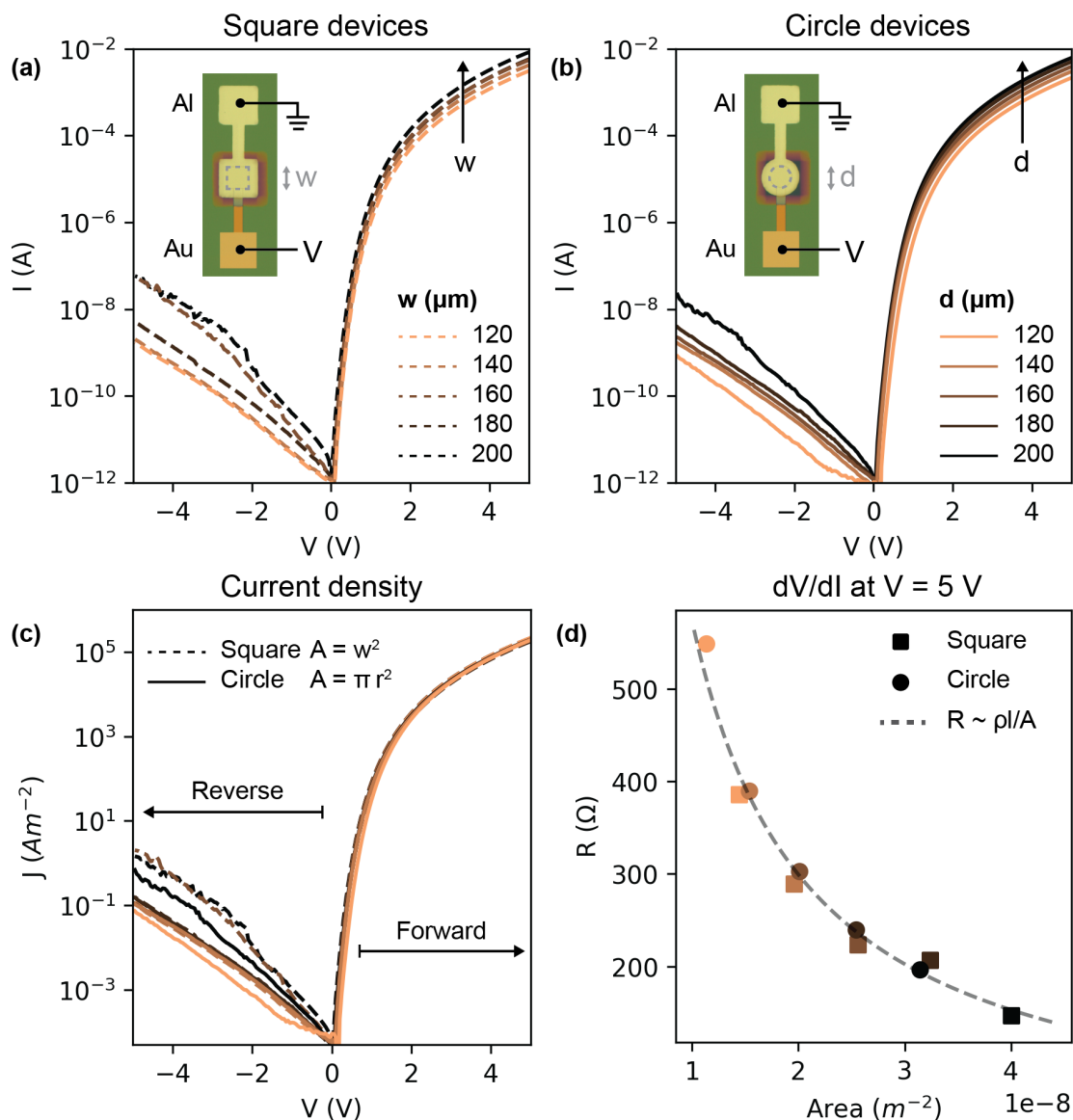
Electrical characterization

Figure 67: (a) IV characteristics of the square shaped devices. The inset shows the optical microscope image of a representative device with a width $w = 120\,\mu m$. The voltage V is applied to the bottom Au electrode, while the top Al electrode is grounded. (b) IV characteristics of the circle shaped devices. The inset shows the optical microscope image of a representative device with a diameter $d = 120\,\mu m$. (c) Current density of the circle and square devices. (d) Differential resistance $R = dV/dI$ calculated at $V = 5\,V$ vs. device area. The grey dashed line is the resistance $R = 1/G = \rho t/A$, which is obtained from the linear fit of the conductance $G = 1/R = \sigma A/t$.

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Figures 67a-b show the current vs. voltage (IV) characteristics of the vertical Au-Pentacene-Al devices with square shaped and circular electrodes, respectively. The insets show that the voltage V is applied to the bottom Au electrode, while the Al electrode is grounded. The traces shows the typical rectification behavior of Schottky diodes with an exponential increase of the current with a positive applied voltage. When a negative voltage is applied, the devices show small leakage current increasing with the reverse voltage. The work functions of Al and Au are $W_{Al} = 4.2\,\text{eV}$ and $W = 4.9\,\text{eV}$, while the HOMO energy level of Pentacene is $E_{HOMO} = 5.1\,\text{eV}$.[1,161] Accordingly, we expect a low injection barrier at the Au electrode of roughly $0.3\,\text{eV}$ and a high injection barrier at the Al electrode of about $0.9\,\text{eV}$. Thus, Au can be considered as the hole injecting electrode and Al the the hole blocking electrode. Since the Pentacene film is only $100\,\text{nm}$ thick, we can safely assume that the depletion region extends over the entire thickness of the device (also at thermal equilibrium).[161] As a result, the voltage drops linearly over the whole structure and the energy diagram of the device can be illustrated as shown in Figure 68. We observe that the magnitude of the current scales with the diameter and width of the devices, while the current density is the same for all devices, as shown in Figure 67c. The devices show a rectification ratio $RR = J(5\,\text{V})/J(-5\,\text{V}) \approx 1 \times 10^6$ and a relatively high current density of approximately $1 \times 10^5\,\text{Am}^{-2}$. Figure 67d shows the differential resistance $R = dV/dI$ as a function of the device area A. It is worth noticing that the resistance of both square and circle devices scales as $R \approx 1/A$. Thus, the geometrical shape of the metal electrodes, which could affect the distribution of the electrical field at the edges and between the electrodes, is not relevant at this scale. The resistivity $\rho = 52.2\,\Omega\,\text{m}$ and conductivity $\sigma = 1.92 \times 10^{-2}\,\text{S}\,\text{m}^{-1}$ are obtained from the fit of the conductance $G = \sigma A/t + C$, where A is the area of the device, $t = 120\,\text{nm}$ is the thickness of the Pentacene film and C is constant. This results in $G = 1.596 \times 10^5 A + 1.498 \times 10^{-4}$, while the plotted dashed line in Fig. 67d is $R = 1/G$. The residual sum of squares of the fit errors is $G_{RSS} = 4.469 \times 10^{-7}$.
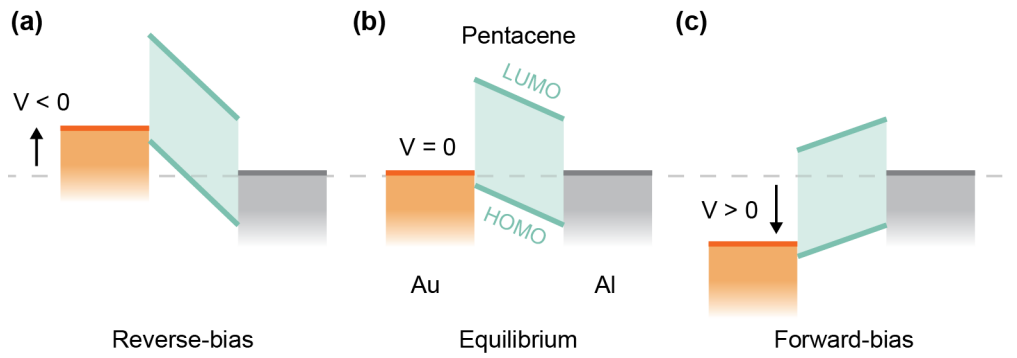
Figure 68: Energy diagram of the Au-Pentacene-Al structure. (a) Reverse-bias regime ($V < 0$). The charge carrier density injected at the Au electrode is low and the current is negligible. (b) Thermal equilibrium. The OSC is fully depleted. (c) Forward-bias regime ($V > 0$). At low positive voltages, the current is limited by the charge injection at the Au electrode. At higher positive voltages (higher than flat-band condition), the current is bulk-limited.

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List of publications

- **Oswald, J.**; Beretta, D.; Stiefel, M.; Furrer, R.; Vuillaume, D.; Calame, M. Complementary Inverter Based on C60 and Pentacene Doped Graphene Field Effect Transistors on SiO$_2$. *Accepted for publication. IEEE Nanotechnology Materials and Devices Conference (NMDC). 2023.*

- **Oswald, J.**; Beretta, D.; Stiefel, M.; Furrer, R.; Vuillaume, D.; Calame, M. Field- and Thermal-Emission Limited Charge Injection in Au-C60-Graphene van der Waals Vertical Heterostructures for Organic Electronics. *ACS Appl. Nano Mat. 2023*, acsami.2c13148. `https://doi.org/10.1021/acsanm.3c01090`.

- Mansour, M. D.; **Oswald, J.**; Beretta, D.; Stiefel, M; Furrer R.; Calame, M.; Vuillaume, D. Nanoscale electronic transport at graphene/pentacene van der Waals interface. *RSC Nanoscale 2023*. `https://doi.org/10.1039/D2NR06682C`.

- **Oswald, J.**; Beretta, D.; Stiefel, M.; Furrer, R.; Vuillaume, D.; Calame, M. The Effect of C60 and Pentacene Adsorbates on the Electrical Properties of CVD Graphene on SiO$_2$. Nanomaterials 2023, 13 (6), 1134. `https://doi.org/10.3390/nano13061134`.

- **Oswald, J.**; Beretta, D.; Stiefel, M.; Furrer, R.; Romio, A.; Mansour, M. D.; Vuillaume, D.; Calame, M. Charge Transport Across Au–P3HT–Graphene van Der Waals Vertical Heterostructures. *ACS Appl. Mater. Interfaces 2022*, acsami.2c13148. `https://doi.org/10.1021/acsami.2c13148`.

- Schmuck, O.; Beretta, D.; Furrer, R.; **Oswald, J.**; Calame, M. A Method to Fabricate Nanoscale Gaps in Graphene Nano-Constrictions by Electrical Breakdown. *AIP Advances* **2022**, *12* (5), 055312. `https://doi.org/10.1063/5.0087564`.

- van Delft, M. R.; Wang, Y.; Putzke, C.; **Oswald, J.**; Varnavides, G.; Garcia, C. A. C.; Guo, C.; Schmid, H.; Süss, V.; Borrmann, H.; Diaz, J.; Sun, Y.; Felser, C.; Gotsmann, B.; Narang, P.; Moll, P. J. W. Sondheimer Oscillations as a Probe of Non-Ohmic Flow in WP$_2$ Crystals. *Nat Commun* **2021**, *12* (1), 4799. `https://doi.org/10.1038/s41467-021-25037-0`.

List of presentations

- 23.10.2023, IEEE Nanotechnology Materials and Devices Conference (NMDC), Paestum, Salerno, Italy. Oral contribution: Complementary Inverter Based on C60 and Pentacene Doped CVD Graphene Field Effect Transistors on SiO_2.

- 29.11.2022, Empa PhD Symposyum on "Emerging Technologies Recent advances, current challenges and outlook", Dübendorf, Switzerland. Poster contribution: Hybrid Van der Waals heterostructures for vertical organic transistors.

- 09.09.2022, Swiss Nanoscience Institute (SNI) annual meeting. Oral contribution: Graphene-organic semiconductor interfaces for vertical organic transistors.

- 29.08.2022, Empa PhD Seminar, St. Gallen, Switzerland. Oral contribution: Hybrid Van der Waals heterostructures for vertical organic transistors.

- 01.12.2021, International Meeting on Molecular Electronics (ElecMol), Lyon, France. Poster contribution: Graphene-organic semiconductor structures for vertical organic transistors.

- 09.09.2021, Swiss Nanoscience Institute (SNI) annual meeting, Lenzerheide, Switzerland. Poster contribution: Graphene-organic semiconductor structures for vertical organic transistors.

- 22.01.2021, Swiss Nanoscience Institute (SNI) winter school, online. Poster contribution: Hybrid Van der Waals heterostructures for vertical organic permeable base transistors.